DUAL RAIL, LOW POWER ASYNCHRONOUS PIPELINE WITH PARTIAL CHARGE REUSE MECHANISM

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ABSTRACT

Here a new type of high throughput asynchronous pipeline structure is proposed. The partial charge reuse (PCR) mechanism is added to the Self Precharge (SP) circuit, which reduces the power consumption. Each pipeline stage consists of a functional block, a completion detector, and an aC element. . Each pipeline stage consists of a functional block, a completion detector, and an aC element. An asymmetric C (aC) element is used to combine the two control signals, which are used to evaluate and precharge a stage. Because of the aC element, the pipeline is able to remove one of the important timing constraints present in lookahead pipelines (LP). Since the SP signal is coming from the same stage without altering the functionality of the signal, the wiring load of handshaking signals between two stages is maintained minimum. The PCR mechanism controls charge reuse between two pipeline stages. It reduces the energy dissipation.

Keywords: Asynchronous pipeline, dual-rail logic, dynamic logic,fine-grain pipelining, PCR mechanism

I. INTRODUCTION

The speed of VLSI circuits increases as the feature size of transistor decreases. To satisfy the ever growing industrial requirements, pipelining can be further employed to enhance the speed. Pipelining can be either synchronous or asynchronous. In synchronous circuit design, a globally distributed clock controls and updates all the memory elements such as flip-flops [1] and latches at the same time. The period of the clock is designed by considering the combinational logic delay, setup time of the memory elements, and the process, voltage, and temperature variations.

Synchronous circuit designs are less complex when compared with asynchronous circuit designs. Asynchronous pipeline can result in many efficiencies, including no synchronization overhead and uniform performance targets. [2].

An asynchronous, or clockless, circuit style [3] was chosen for several reasons. First, while synchronous designers are currently capable of achieving multi-gigahertz clock distributions, the task involves the ever-increasing challenges of design time, verification effort, clock skew, and power management, and interfacing with different timing domains. Second, since an asynchronous pipeline has no global clock, it has a natural elasticity. The number of data items in the pipeline, and the speeds of the external interfaces, can vary dynamically. As a result, the pipeline can gracefully interface with environments operating at different rates, including those subject to dynamic voltage scaling, thus facilitating modular and reusable design. In asynchronous circuits, different functional blocks communicate using local handshaking protocols [4]–[6].

Asynchronous pipelining has several advantages over synchronous pipelining, such as: 1) no global clock distribution problem; 2) no clock skew; and 3) lower power consumption. Further, an asynchronous design can support variable data rate because of the local handshaking signals, and thus possess natural elasticity and hence can automatically adapt to the environment [7]. But, it also has some disadvantages such as: 1) difficulty in testing; 2) design is unsupported by most of the EDA tools; and 3) difficulties in interfacing with synchronous environments. Asynchronous designs have started to replace their synchronous counterparts and recent decades have witnessed many asynchronous products [8]–[12].

If efficient asynchronous communication can be designed, three significant benefits arise. First, each module can be designed for its best frequency and power. Second, the ability to interconnect components with different frequencies will be vastly enhanced resulting in higher design reuse, faster time to market, and easier ability to customize designs. Third, the ability of the asynchronous designs to adapt themselves to physical properties can lead to more robust design.

II. BACKGROUND: DUAL-RAIL ASYNCHRONOUS PIPELINES

This section briefly explains Williams' PS0 pipeline and different lookahead pipelines (LP). These pipelines as well as the SP pipeline use dual rail time -constrained protocol. The other high-speed asynchronous pipelines that exist in the literature are GasP pipeline and IPCMOS pipeline . But they use single rail two-sided timing constraints. Moreover, GasP and IPCMOS pipelines use complex signal schemes and controlling circuits.

A. WILLIAMS' PS0 PIPELINE

In Williams' PS0, each pipeline stage is composed of a dual rail functional block and a completion detector. For PS0, the cycle time is given by,

$$T_{cycle} = 3T_{eval} + 2T_{cd} + T_{prech}$$

where Tcd is the completion detector delay and Tprech is the time taken by a stage to precharge.

B. LOOKAHEAD PIPELINES

LP took PS0 as the basic building block and achieved higher performance by optimizing the protocol.

1) LP3/1 Pipeline: Unlike PS0, LP3/1 combines two signals to get the pre charging (PC) input of a stage. Even though the NAND gate directly comes in the critical path, it still offers better performance than PS0.

2) LP2/2 Pipeline: The architecture of LP2/2 pipeline is shown in Fig. 1. Each stage consists of a functional block and a completion detector, which are shown in Fig. 2. The completion detector is an asymmetric C-element (aC) [16], [18], which is placed before the associated stage, so that it generates "done" signal in parallel with the evaluation of the functional block.

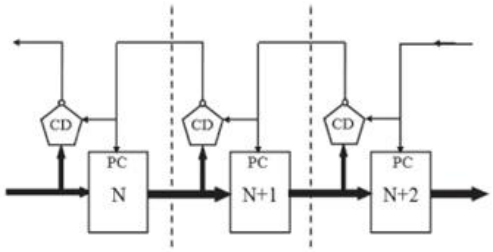

Fig. 1. Structure of LP2/2 pipeline.

3) LP2/1 Pipeline: It is the fastest dual rail lookahead pipeline[18]. It combines optimizations of both LP3/1 and LP2/2 to get a better performance.

C. ENHANCED LP

LP structures require more wiring load and they require two control signals to and from the environments.

To overcome these issues, enhanced LP3/1 and LP2/1 implementations were introduced.

1) Enhanced LP3/1 Pipeline: The architecture of enhanced LP3/1 pipeline is shown in Fig. 3. The pipeline protocol remains the same as that of basic LP3/1, but because of the modified structure, only the adjacent stages are communicating directly. Thus, the pipeline can easily communicate with the environment and the interstage control signals are reduced.

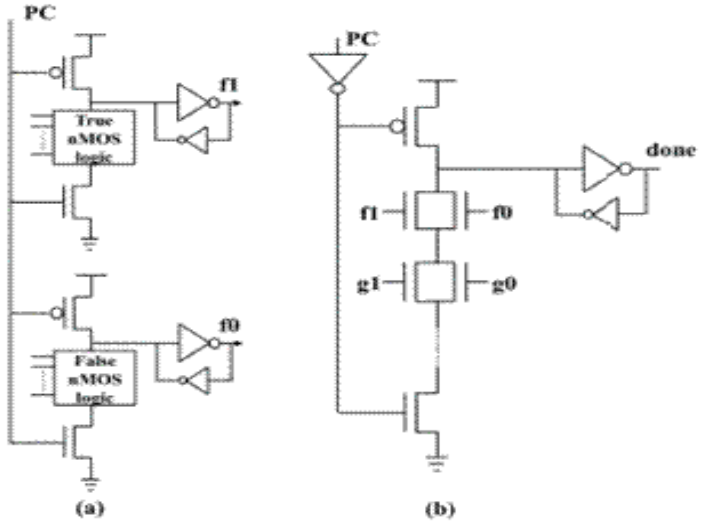

Fig. 2. Dual-rail logic. (a) Functional block. (b) Completion detector.

2) Enhanced LP2/1 Pipeline: The architecture of enhanced LP2/1 pipeline shown in Fig. 4 is implemented by restructuring the basic LP2/1 pipeline in the same way as enhanced LP3/1 was implemented from basic LP3/1

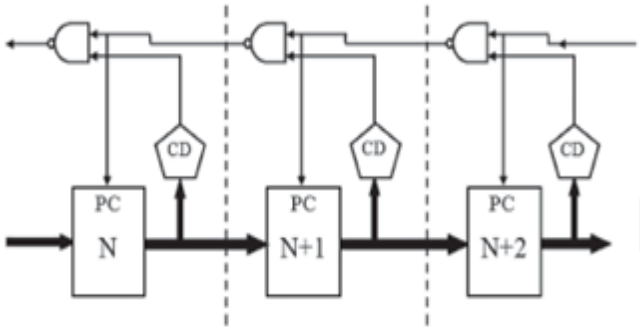

Fig. 3. Structure of enhanced LP3/1 pipeline.

The main disadvantage of PS0 pipeline is its poor throughput. The second data token has to wait for the completion of all six events in "(2)." The LP pipelines improve throughput at the expense of greater wiring load and more timing constraints.

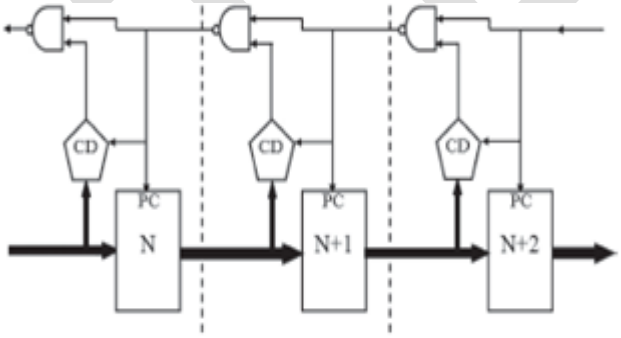

Fig. 4. Structure of enhanced LP2/1 pipeline.

III. SP PIPELINE

A. PIPELINE STRUCTURE

The structure of a SP pipeline is shown in Fig. 5. Each pipeline stage consists of a functional block, a completion detector, and an aC element. The functional block shown in Fig. 2(a) is same as that used in Williams' PS0 pipeline and LP

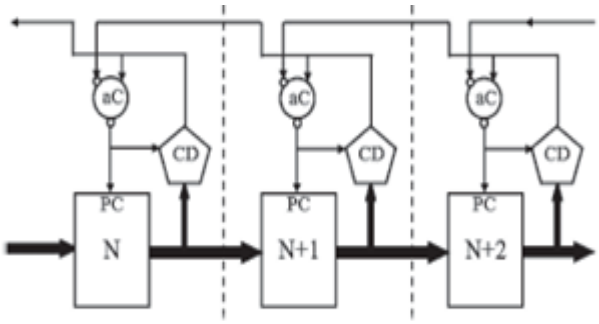

Fig. 5. Structure of SP pipeline.

The completion detector shown in Fig. 2(b) is the same one used in LP2/2 and LP2/1 pipelines. This completion detector has less area, delay, and power consumption compared to the symmetric C element used in the PS0 and LP3/1 pipelines [18]..

Completion detectors are placed before the functional block in LP2/2 and LP2/1 so that they can anticipate the completion of evaluation. In SP topology, completion detector is moved and placed just after the previous stage, so it can be included in the previous stage without any change in the functionality. This results in reduced interstage wiring load. Now only one control signal is given to the previous stage like PS0 and enhanced LP, which is important for the future technologies.

B. PCR MECHANISM

There are two main differences between SP-PCR and SP w/o PCR. First, SP-PCR employs the PCR unit PCRi+1 to control charge reuse between pipeline stages N and N+1. By using this mechanism we can reduce the power consumption of proposed circuit without performance degrading.

In SP-PCR uses a aC-element to control the power node Vpi of the associated SP gates. The aC-element offers the advantage that an SP gate can achieve early discharging if its outputs are no longer required, without waiting for the next empty token to arrive at this stage. In the PCRi+1 unit, transistor is used as a diode, which allows the current to flow only in the direction from Vpi to Vpi+2, and transistor is used as a switch, which is turned on when charge reuse is activated.

The pre charging of a stage is associated with the evaluation of the next stage. In SP pipeline, the completion detector's "done" signal is used to pre charge the completion detector as well as the functional block. Hence, it is named SP pipeline. Because of the use of SP protocol, no additional signals are taken from the next stage. This is one important feature of the SP protocol. Now the completion detector does not need to wait for the pre charge signal from the next stage, but it is driven to pre charge state by its own "done" signal.

IV. SIMULATION RESULTS

All the custom cells were designed in identical fashion. Identical completion detectors were used in LP2/2, LP2/1, and SP. Similarly, the completion detectors of PS0 and LP3/1 are identical to each other. The method of logical effort [21] is used to calculate the transistor sizes and all the discrete components used in the designs are of same transistor size

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Power Results
vvdd from time 0 to 1e-007
Average power consumed -> 4.707026e-004 watts
Max power 1.128030e-002 at time 2.00007e-008
Min power 3.701174e-004 at time 8.01953e-008
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Fig: 7 Output Power of SP

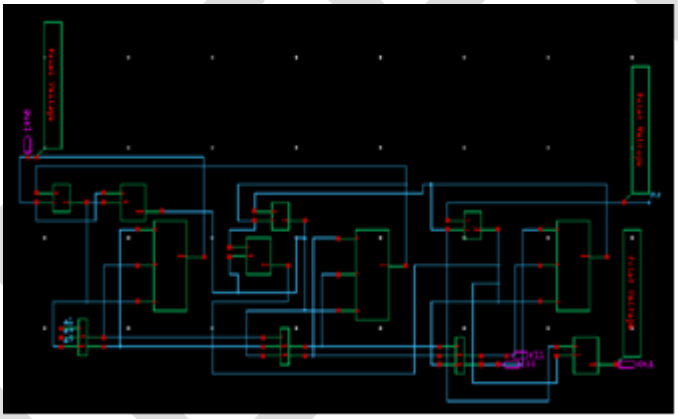

Fig:8 Schematic of SP with PCR mechanism

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Power Results
vvdd from time 0 to 1e-007
Average power consumed -> 2.805205e-004 watts
Max power 1.131426e-002 at time 1.00007e-008
Min power 1.672959e-004 at time 0
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Fig: 9 Output Power of SP

Enhanced LP3/1 has the highest power consumption and area, followed by PS0, while LP2/2 has the lowest power consumption and area. Enhanced LP2/1 and SP pipeline have almost same

area and power consumption. But because of the resetting logic and the feedback weak inverter used in aC element of SP pipeline, it consumes slightly higher power, which is not required for the NAND gate in LP2/1.

V. CONCLUSION

The proposed SP pipeline is able to deliver multigigahertz throughput. The SP pipeline uses novel protocol and modified structure to optimize the performance. The use of aC element removes the important safe takeover timing constraint of the LP family, making the pipeline simpler to design.

The proposed SP pipeline offers the highest throughput (2.227 giga data items/s) compared to the other pipelines discussed in this brief. The SP pipeline offers more than twice (114.03%) the throughput of Williams' PS0 and 21.38% improvement over the best lookahead pipeline (LP2/1), while maintaining the same per-stage forward latency.

Area and power consumption are comparable with LP2/1 pipeline. The SP pipeline has less area and power consumption compared to PS0 pipeline. SP pipeline preserves advantages (which are common to the PS0 and LP family) like low latency, high robustness, low power, avoidance of explicit latches, etc., compared to its synchronous counter parts.

The partial charge reuse (PCR) mechanism is incorporated in the Self Precharge (SP) circuit. The PCR mechanism controls charge reuse between two pipeline stages. It reduces the energy dissipation. With the PCR mechanism, part of the charge on the output nodes of a discharging ECRL logic gate can be reused to charge another ECRL logic gate.

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