Comparative Study of Multicarrier PWM Techniques for a 33-level MMC

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***Abstract*—** This paper presents the simulation of three phase 33-level modular multilevel cascade inverter based on double-star chopper-cell (DSCC). The multicarrier PWM techniques such as Phase disposition PWM (PDPWM), Phase opposition disposition PWM (PODPWM), Alternate phase opposition disposition PWM (APODPWM), and Phase shift PWM (PSPWM) is employed and a comparative study is done based on the spectral quality of the load voltage and load current waveforms. Simulation has been carried out for modulation index 1.0 using MATLAB/Simulink and the results are verified.

Keyword- Modular Multilevel Converter (MMC), Double star chopper cells (DSCC), Multicarrier PWM (MCPWM), Total harmonic distortion (THD).

I.INTRODUCTION

Modular multilevel converters have great potential in high-power applications, such as dc interconnections, dc power grids and off-shore wind power generation are in need of accurate power flow control and high efficiency power conversion in order to reduce both their operating costs and their environmental impact. High power converters for utility applications require line-frequency transformers for the purpose of enhancing their voltage or current rating. The use of line-frequency transformers, however, not only makes the converter heavy and bulky, but also induces the so-called dc magnetic flux deviation when a single-line-to-ground fault occurs.

Multilevel converters are used for achieving medium-voltage power conversion without transformers. Two of the representatives are: 1) the diode-clamped multilevel converter (DCMC); 2) the flying-capacitor multilevel converter (FCMC). The three-level DCMC or a NPC converter has been put into practical use. If a voltage-level number is more than three in the DCMC, inherent voltage imbalance occurs in the series-connected dc capacitors, thus resulting in requiring an external balancing circuit (such as a buck–boost chopper) for a pair of dc capacitors. Furthermore, a significant increase in the clamping diodes required renders assembling and building of each leg more complex and difficult. As for the FCMC, the high expense of flying capacitors at low carrier frequencies (say, lower than 1 kHz) is the major disadvantage of the FCMC.

The characteristics of the MMC is low switching losses due to a considerably lower switching frequency (fs ≈3f1), compared to a 2-level equivalent. Apart from the lower switching frequency, the quality of the output voltage waveform is higher. Thus smaller and simpler harmonic filters are required. A short circuit at the DC-bus will not discharge the storage capacitors therefore fault recovery is very fast. The MMC provides simplicity of design and control, as well as scalability to various voltage and or power levels. Moreover, MMC has the potential to improve the reliability, as a faulty module can be bypassed without significantly affecting the operation of the whole circuit.

However, the star/delta-configured MMC topology has no common dc-link terminals. As a result, it has no capability of achieving dc-to-ac and ac-to-dc power conversion although it can control active power back and forth between the three phase ac terminals and the floating dc capacitors. This means that the star/delta configured MMC topology is not applicable to industrial motor drives, but it is suitable for STATCOMs and energy storage systems.

II. STRUCTURE OF MMC

Fig. shows the single phase and three phase equivalent circuit of n-level MMC configuration, The converter has one leg comprises of two arms including the upper arm and lower arm, with each arm having n/2 sub modules (SM) and two non coupled buffer inductors and an equivalent resistor. Each sub module disturbs operation or generate overvoltage for the semiconductors. The buffer inductor can limit the AC-current, whenever the DC-Bus is short circuited (fault condition) and it act as

passive filter during normal condition. The DC Link of MMC is connected to module comprises of two switches and one sub module capacitor. The two non coupled buffer inductors are inserted into the arms, since they do not selected with the same phase, the method is known as high-voltage sources depending on the working purpose of the converter. The output of the converter is the connection point of the upper and lower connection point of the upper and lower arm which is connected to RL load.

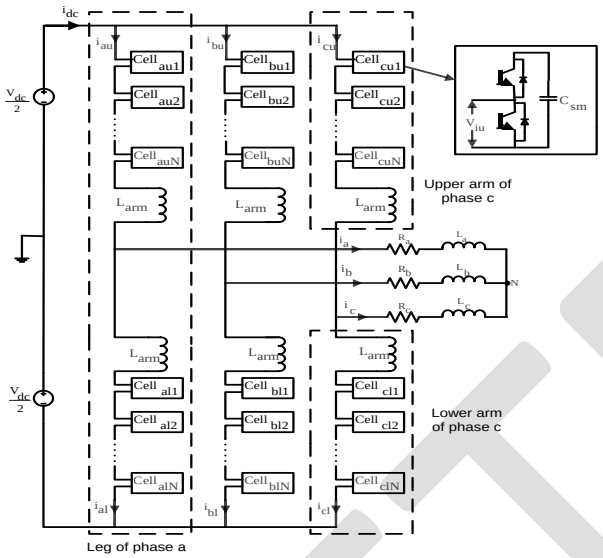

Fig. 1 Three phase n-level MMC

III.MULTI-CARRIER PWM STRATEGIES FOR MODULAR MULTILEVEL CONVERTER

Multi-Carrier PWM strategies is widely used, because it can be easily implemented to low voltage modules. MCPWM be classified as level shifted PWM (LS-PWM) and Phase shifted PWM (PS-PWM) techniques. The level shifted PWM (LS-PWM) are Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD). In general the amplitude modulation index (m_a) is defined as the ratio of amplitude of the reference sine wave (A_r) to the amplitude of the carrier wave (A_c). The frequency modulation index (m_f) is defined as the ratio of frequency of the carrier wave (f_c) to the frequency of the reference sine wave (f_r).

1) *Phase Disposition PWM (PDPWM)*

In this method all the carriers above and below zero reference line are in same phase. The PDPWM is the widely used strategy for MMC and conventional multilevel inverters because it provides load voltage and current with lower harmonic distortion. The converter is switched to + Vdc / 2 when the sine wave is greater than both carriers, the converter switches to +Vdc / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carriers, the converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier, the converter switches to - Vdc / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers and the converter is switched to - Vdc / 2 when the sine wave is less than both carrier waveforms.

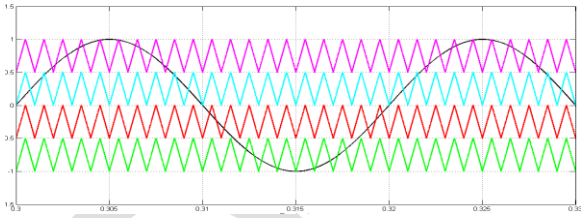

Fig.2 carrier arrangement for PDPWM strategy ($m_{a=1.0}$, $m_{f=20}$)

2) *Phase opposition disposition PWM (PODPWM)*

In this method all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes). But all the carriers above the zero value reference are in phase among them but in opposition (180 degrees phase shifted) with those below. The converter switching is similar to the PDPWM strategy. Based on the converter switching the MMC has different levels of voltage.

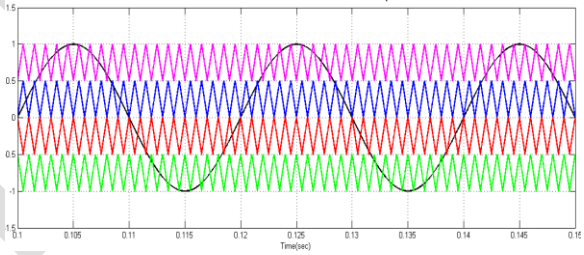

Fig.3 carrier arrangement for PODPWM strategy ($m_{a=1.0}$, $m_{f=20}$)

3) *Alternate phase opposition disposition PWM (APODPWM)*

In this method all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes). All the carriers have180_0 phase shift between them.

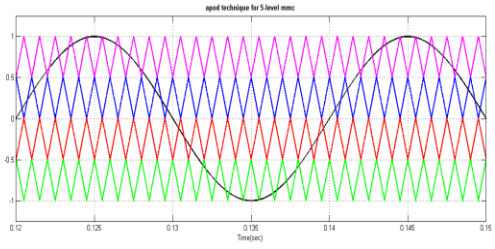

Fig.4 carrier arrangement for APODPWM strategy ($m_{a=1.0}$,$m_{f=20}$)

The converter switching is similar to the PDPWM strategy. Based on the converter switching the MMC has different levels of voltage.

4) *Phase Shift PWM (PSPWM)*

The phase shift multicarrier PWM technique is another type of multicarrier PWM strategy and has its performance parameters closest to PDPWM strategy. It uses four carrier signals of the same

amplitude and frequency which are shifted by 90 degrees to one another.

The carrier waves are phase shifted so that the switching instants of different sub modules are offset in time, thus reducing the harmonics in the output voltage. This technique ensures substantial reduction in losses as each sub module switches at only a fraction of the overall switching frequency.

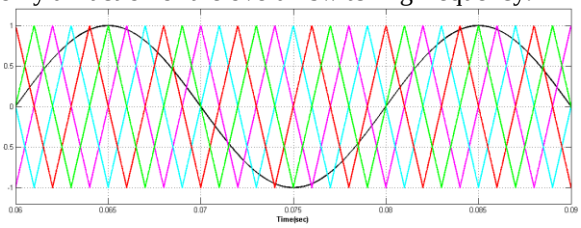

Fig.5 carrier arrangement for PSPWM strategy ($m_{a=1.0}$, $m_{f=20}$)

Even though PSPWM is easy to implement the control becomes complex as the number of modules increases. This can be overcome by lowering the switching frequency for individual sub modules but it leads to voltage fluctuations in the sub module voltages.

IV. SIMULATION RESULTS

Simulation of three phase 33-level Modular Multilevel Converter is done. The output phase voltage and phase current waveforms of three phase 33-level MMC as shown in fig. 6, 7 and FFT analysis of output voltage and current for various PWM strategies with modulation index 1.0 is done. The output waveforms of 33-level MMC is

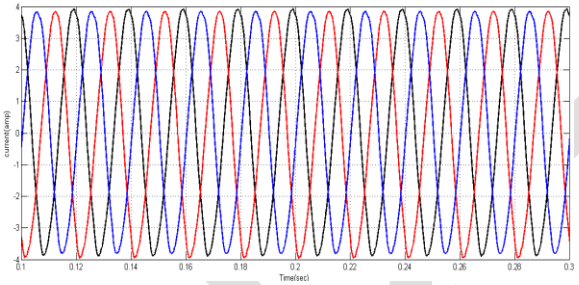

Fig.6 Simulated phase voltage of 33-level MMC for MI-1.0

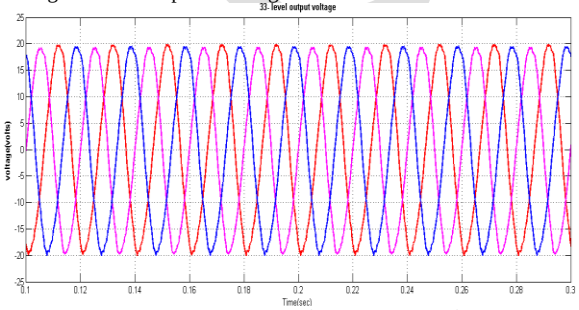

Fig.7 Simulated phase current of 33-level MMC for MI-1.0

The THD of output voltage and current of 33-level MMC with PDPWM strategy for MI-1.0 using FFT analysis are of 6.08% and 5.83%.

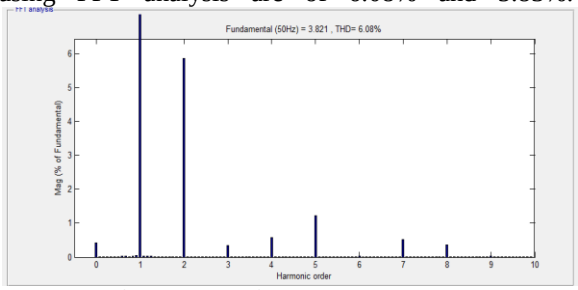

Fig. 8: THD of phase voltage for 33-level MMC with PDPWM

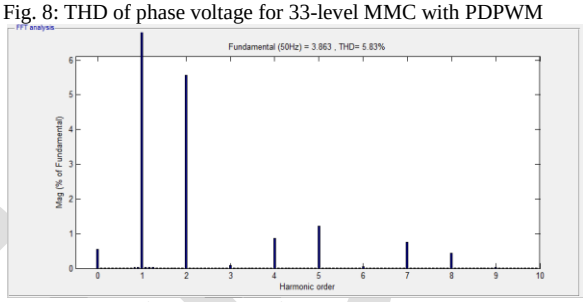

Fig. 9: THD of phase current for 33-level MMC with PDPWM

The THD of output voltage and current of 33-level MMC with PODPWM strategy for MI-1.0 using FFT analysis are of 6.98% and 6.77%.

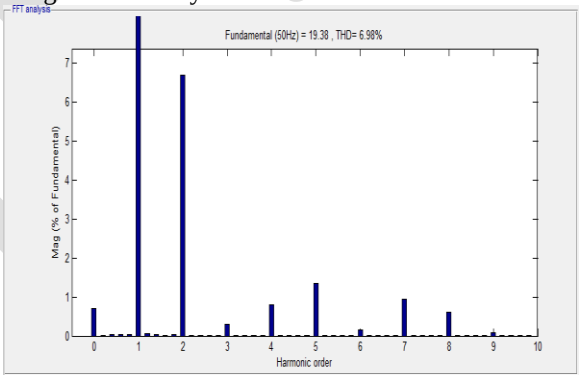

Fig. 10: THD of phase voltage for 33-level MMC with PODPWM

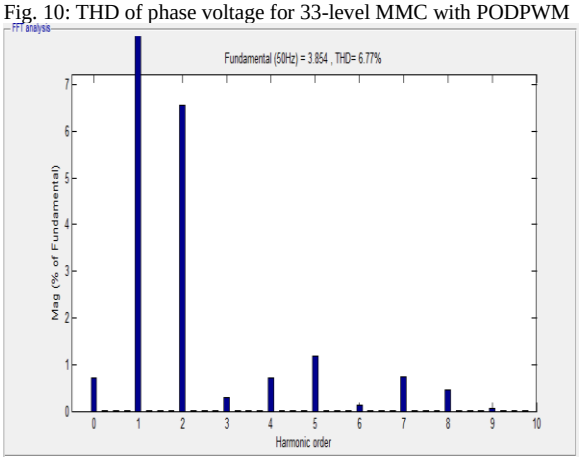

Fig. 11: THD of phase current for 33-level MMC with PODPWM

The THD of output voltage and current of 33-level MMC with PODPWM strategy for MI-1.0

using FFT analysis are of 6.53% and 5.83%.

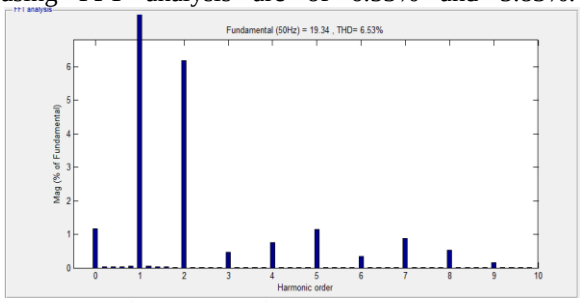

Fig.12: THD of phase voltage for 33-level MMC with APODPWM

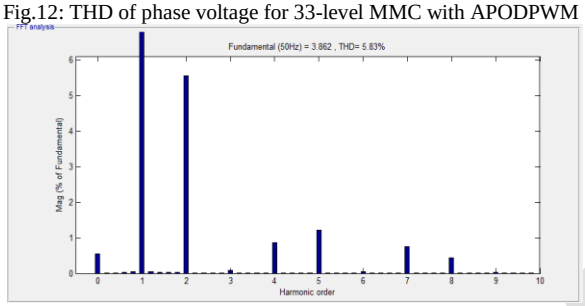

Fig.13: THD of phase current for 33-level MMC with APODPWM

The THD of output voltage and current of 33-level MMC with PSPWM strategy for MI-1.0 using FFT analysis are of 6.29% and 6.09%.

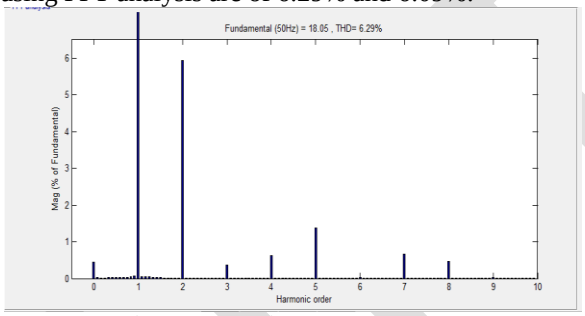

Fig. 14: THD of phase voltage for 33-level MMC with PSPWM

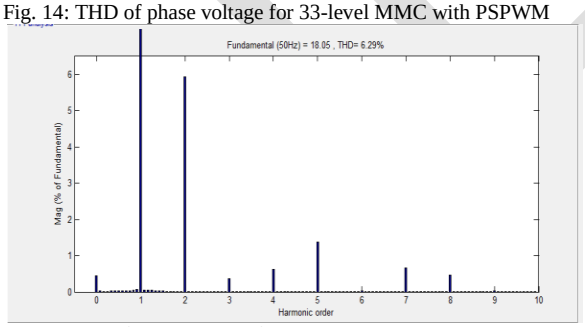

Fig.15 THD of phase current for 33-level MMC with PSPWM

Cumulative comparison between the various PWM techniques (PD, POD, APOD &PSPWM) with modulation index 1.0 for 33-level MMC is as follows.

PWM technique	33-level MMC with MI-1.0	
	V	**I**
PDPWM	6.08	5.83
PODPWM	6.98	6.77
APODPWM	6.53	5.83
PSPWM	6.29	6.09

Table.1 comparison of THD of output voltage and current of 33-level MMC

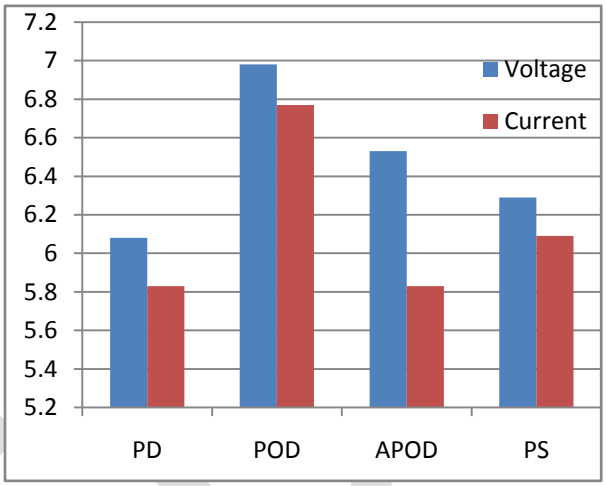

Fig. 16 cumulative comparison of THD of various PWM techniques of 33-level MMC

From the cumulative comparison of THD's of output voltage and current of various PWM techniques of 33-level MMC, PDPWM technique is better one compared to remaining techniques. Whereas the THD's of PSPWM technique is nearer to the PDPWM technique. Because of this reason in general practical applications PDPWM & PSPWM techniques are mostly used.

V.CONCLUSION

In this paper, three phase 33-level modular multilevel inverter based on double star chopper cells configuration employing PDPWM, PODPWM, APODPWM and PSPWM multicarrier PWM strategies with RL load of modulation index 1.0 is simulated using Matlab/Simulink software. The detailed comparison is done for the MMC-DSCC employing multicarrier PWM strategies based on the load phase voltage, load phase current and Total Harmonic Distortion. The PDPWM strategy produces the Total Harmonic Distortion (THD) of output phase voltage and output phase current for 33-level MMC with modulation index 1.0 are of 6.08% and 5.83%. Thus PDPWM strategy is the best method providing the better load voltage with low THD compared to other. From the above values, by increasing the number of levels gradually the output sinusoidal waveform will be improved with reduction in the total harmonic distortion.

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