SIMULATION OF AN ELECTRONIC VOTING MACHINE WITH FPGA

R.AKSHAYA [#1], M.NITHYA [#2], D.SAINATH REDDY [#3], SNEHA SUSAN ABRAHAM [#4]

[#1]Department of Electronics and Communication engineering, Saveetha School of Engineering, Saveetha University, Chennai-602105, phone no: +91 9789817114

[#1]Department of Electronics and Communication engineering, Saveetha School of Engineering, Saveetha University, Chennai-602105, phone no: +91 8940013987

[#1]Department of Electronics and Communication engineering, Saveetha School of Engineering, Saveetha University, Chennai-602105, phone no: +91 9788378753

[#1]Department of Electronics and Communication engineering, Saveetha School of Engineering, Saveetha University, Chennai-602105, phone no: +91 9789817114

ABSTRACT

This paper gives the overview of the simulation of an electronic voting machine, the control unit of the device being FPGA. A simple database has been implemented with the registry to ensure and validate the eligibility of the voters. The conventionally used ballot unit is accessible to voters for casting their votes while the control to permit the voters eligible resides with the presiding officer. The FPGA control unit provides an efficient system of memory usage.

Keywords: EVM, FPGA, VHDL

Corresponding Author: R.Akshaya

INTRODUCTION

India after independence on becoming a democratic country needed a voting policy and a reliable system to execute its elections all around the country. At first the simple ballot box method of casting votes were practised. But soon, this method was seen very inefficient as:

1) Printing of ballot papers for such a huge population was seen difficult and required much time.
2) Citizens not having proper knowledge to vote recorded invalid votes, as the probability of stamp ink on the boundary or copied to other candidates were high.
3) The number of ballot boxes to be maintained and secured until the result day was huge.
4) High requirement of manpower for counting the votes.
5) Time taken to finalize the result was too high.

Thus, there came an urgent need to modernize the system for something that proves way more efficient to cater the needs of this huge population being time efficient and easy to use. Mr.M.B.Haneefa invented and gazetted the electronically operated voting machine (Gazette: 191/Mas/80, 15 October 1980). His original design was exhibited in six cities across Tamil Nadu. Consequently, the EVMs (electronic voting machines) were commissioned in 1989 by Election Commission of India in collaboration with Electronics Corporation of India Limited. The Industrial designers of the EVMs were faculty members of Industrial Design Centre, IIT Bombay. The EVMs were first used in 1998 in the by-election to North Paravur Assembly Constituency in Kerala for a limited number of polling stations. The EVMs mainly consist of two units: Ballot Unit and Control Unit. The ballot unit contains options for casting of votes to any of the candidate contesting in the election. The control unit resides with the presiding officer or the polling officer which is connected to the ballot unit by a 5m cable. Still the EVMs are under the development stage for further innovations and improvements. There are a lot many analyses done on the basic electronic voting machine existing in our country and other countries on the grounds of their security [1-3]. Many simple and fast response electronic voting machines have been proposed of which microcontroller based simple machines are already used throughout the country [4-5]. Recent researches for E-Voting systems propose it to a good choice of future implementation [6-9]. But still their integrity and usability in a country like India has to be surveyed and analysed in terms of ease of use, secure voting, accessibility throughout the country and the system's ability to bear such a huge population.

This paper gives a very realistic usage of the electronic voting machine with an error controlling mechanism of multiple voting from the same voter. The control unit of EVM is realised through VHDL simulation that can be implemented in the Spartan 3E kit FPGA. Since in FPGA, each voted that is casted is of one bit memory, the whole set up becomes memory efficient.

THE EXISTING EVM

The existing electronic voting machine implements a control unit with control signals corresponding to the selection of mode, total, clear, close, authority switch and candidate signal. There are two modes of operation of the control unit, one being the voting mode and the other counting mode. During the elections, the control unit is programmed to work in the voting mode to receive signals for the votes casted against each candidate. The authority switch in the voting mode that is under the control of the presiding officer is a crucial signal that gives permission for the each voter to vote against his/her favourite candidate. After each vote being recorded, the ballot unit get locked in order to avoid errors such as multiple time voting and inappropriate casting. Until the clearance of the next new candidate's eligibility is decided, no further votes have to be recorded. Later after which this authority switch permits and counts the next respective signal from the ballot unit. The counting mode is reserved for the day of result. This caters to total and result signals. These switches are sealed during the day of election to ensure that no wrong usages occur and the result is not manipulated. The ballot unit simply contains the LCD display showing all the candidates contesting and the buttons corresponding to vote for them. The ballot unit is disconnected after the election from the control unit. This calls for an efficient memory usage and security precautions for the control unit. Although this system has reduced a load of manual work, our proposed system helps in further reducing it and increasing the quickness of verification procedures of each vote.

OVERVIEW OF THE SIMULATED MODEL

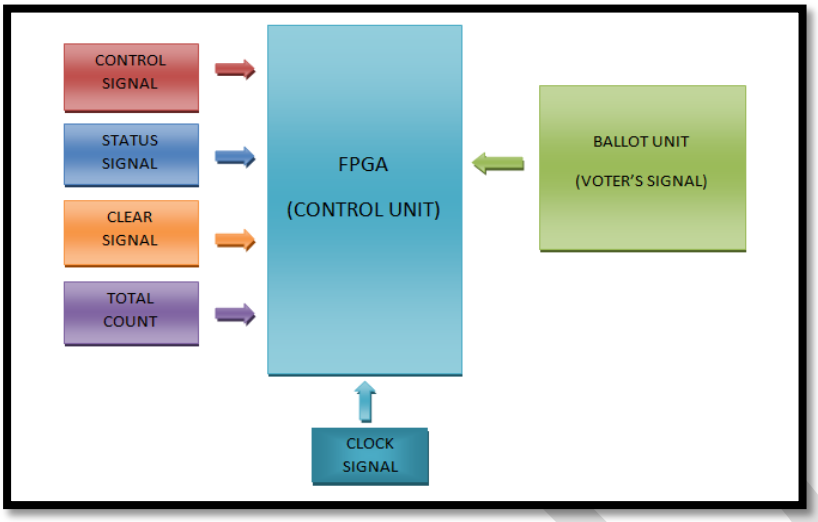

Fig 1: Block diagram depicting the basic blocks of the proposed EVM.

The basic block diagram in Fig 1 gives the brief idea of the functionality of EVM. There are many proposals for the biometric verification of the voter's identity [10-11]. But India to the best of knowledge is not having any near future proposals on implementing such techniques. The Additional database in this electronic voting machine is not that heavy to be implemented as a memory load on the software paradigm. It simply contains a controlling mechanism that stores all the voters eligible and has voted in the respective polling booth the machine is serving. This technique is a primitive idea that provides the serialised number list of all the voters, which can either be extended to a biometric system of verification or by simple checking the voter's electoral number. TABLE 1 gives the complete detail of all the signals used and their functions.

TABLE 1. LIST OF SIGNALs AND ITS FUNCTIONS

SIGNAL NAME	PURPOSE OF SIGNAL	NUMBER OF SUCH SIGNALS	OUTPUT RANGE
CLEAR	To erase previous data	Only one signal.	1-digit Binary value.
CLOCK	Provides timing reference for operations	One signal.	1-digit Binary value.
VOTER'S SIGNAL	Contains the information of the candidate to which vote has been casted.	As many as the number of voters allotted for a polling booth; 20 signals.	For this case, 2-digit binary value giving 4 combinations for 4 candidates.
CONTROL SIGNAL	Monitors eligibility of the voter; default=0; becomes 1 when the voter has voted.	As many as the voter signal; 20 signals.	1-digit binary value.
STATUS SIGNAL	Displays 'VOTED' after each voter has casted the vote. Displays when control signal is 1.	As many as the control signal; 20 signals.	1-digit binary value.

CANDIDATE SIGNAL	Updates and gives information about the vote casted for contesting candidates. Gets updated with each voting.	Equals the number of candidates contesting in the division; 4 signals.	Range of integer values equalling to the total number of voters.
WINNER COUNT	Displays the winner of the election process from time to time.	Only one signal.	ASCII values to depict the winning candidate.

RESULTS

A. MAJOR LOGICAL BLOCKS

The simulated result of the behavioural model containing the total number of votes after all the votes are recorded has been executed using MODELSIM with the means of VHDL codes.

We have segregated the control unit into three major logic blocks:

1) ENTRY BLOCK: This is the functional block that accepts the voter's signals as input. The logical operations done by this block are: a) to increment the total votes gained by the respective candidate if the control signal is not 1, b) to set the control signal of the respective voter to 1 from 0.
2) STOP BLOCK: This block gives the status of each voter, the input to this block being the control signal. When the control signal is set to 1; status of the voter becomes 'VOTED'.
3) COUNT BLOCK: Count Block is the final resultant block that functions for finalizing the winner for whom the maximum vote has been casted. This is however, done and updated after each vote is given and the candidate's count increases.

B. SEQUENCE OF EVENTS

The figures show the order of events, first is to enable the clock signal and run the simulation.

1) Clear is set to 1. This erases all the previous data. And is forced to zero for voting to take place.
2) First vote is casted. It is not mandatory that only Voter 1 should vote first.
3) VOTING OPTIONS: there are 4 candidates set. Hence a 2-digit binary number suffices 4 candidates. 00-First candidate; 01-second candidate; 10-third candidate; 11-fourth candidate.
4) After the voter has exercised his/her vote, the rising edge of the clock pulse set the control signal to 1; default value being 0.
5) The count of the candidate for whom vote has been given is incremented; default value of integer is 0.
6) The above occurs at the first rising edge of the clock pulse. The status signal and the winner counting process can occur only after the control signal is set to 1 and the candidate signal has been updated.
7) Hence, in the successive clock pulse, the status signal respective to the candidate voted becomes 'VOTED'.

8) The winner count displays the winner (winner until the previous clock pulse).
9) The control signals, status signals and winner count signal are internal signals. The next voter can immediately vote in the clock pulse successive to the previous voter.
10) FALSE CASE: If the same voter who has voted already before tries to cast vote again, the present false vote is not counted and valid. This is controlled by the control signal. Once a voter has voted, the control signal becomes 1. This will ensure no further approval of votes from the same person.

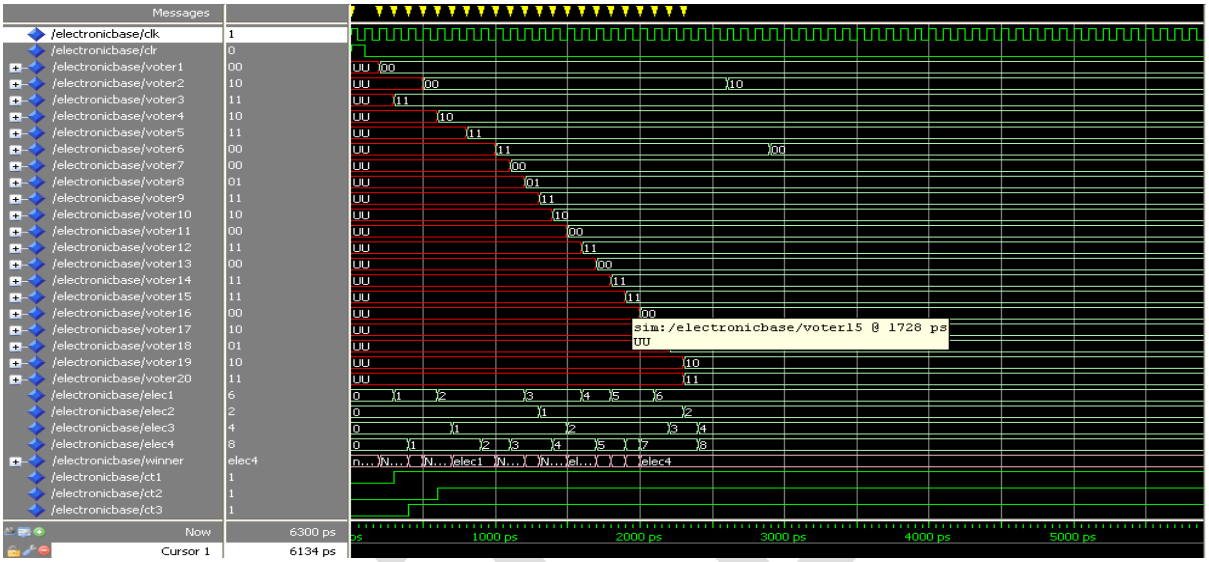

Fig 2: The voter's signals, votes to respective candidates and the winner of the votes from time to time.

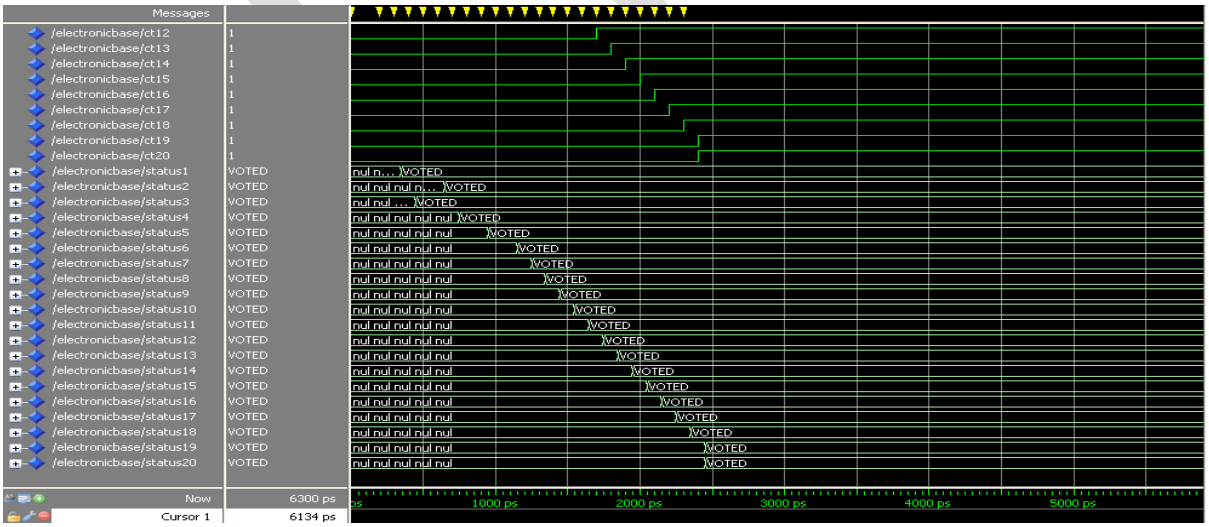

Fig 3: Control signals of all the voters and their status displaying 'VOTED'.

Fig 2 and fig 3 shows the simulated output that contains the entire voters list. In this case, 20 eligible voters is stored. Each voter can cast vote to any of the candidate; in this simulation being 4. When signal '00' is sent, candidate 1 gets the vote; similarly for '01' to candidate 2; '10' for candidate 3; '11' for candidate 4. The first voter has voted for candidate 1. The control signal becomes 1 for voter 1 and the vote count increases by 1 for candidate 1. In the next clock cycle, voter 2 also votes for candidate 1 and similarly all the voters follow.

It is not mandatory for the voters to cast vote in the same order stored. For instance, Voter 3 has voted before voter 2. This list of voters can be stored in advance before the polling starts. Thus, the identity of each of these voters can be verified either through biometric system or by simple through their electoral identity. The Figure 2 also shows that after all the voters have voted, voter 2 and voter 6 are trying to cast multiple votes. Although these signals are sent to the control unit (FPGA), the signals are not counted for results and they are discarded. The control of eliminating multiple votes lies with the control signal and status signal. Fig 4 shows the entry unit, the only external signals to the voting machine are the voter's signals. All the control signals, status signals and winner count and clock signal are of internal type. Fig 5 gives the logical block that changes the status of each voter to 'VOTED' once he/she has voted. The status of the voter depends upon the corresponding control signal. Fig 6 is the final resultant block that display the winner of all the candidates until the before clock pulse. Fig 7 depicts the entire logical connections between all the units interconnected.

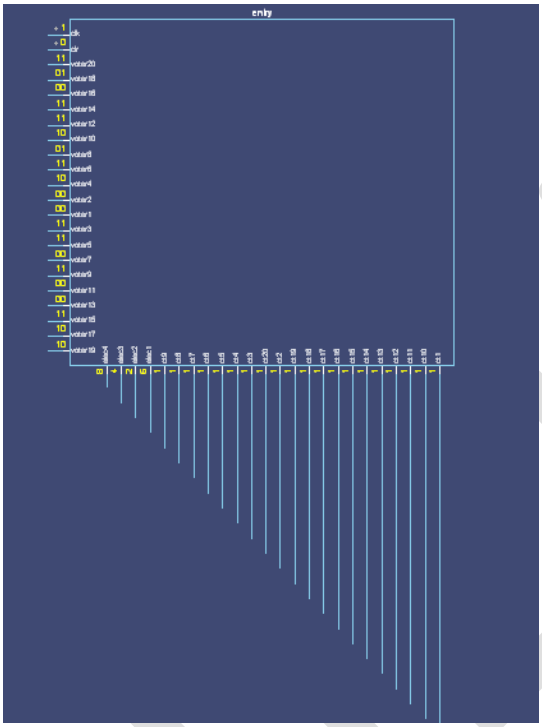

Fig 4: Logical Block of Entry unit with voter's signals as input and control and candidate signals as output displaying the respective signals values.

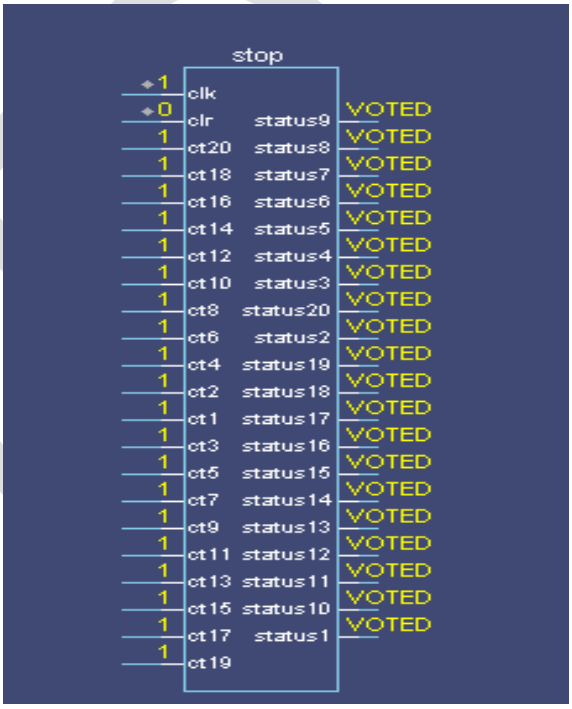

Fig 5: Logical block diagram of Stop unit that displays the status as 'VOTED' and stops each candidate from multiple voting.

Fig 6: Logical block of counting unit that results in the winner of the total votes.

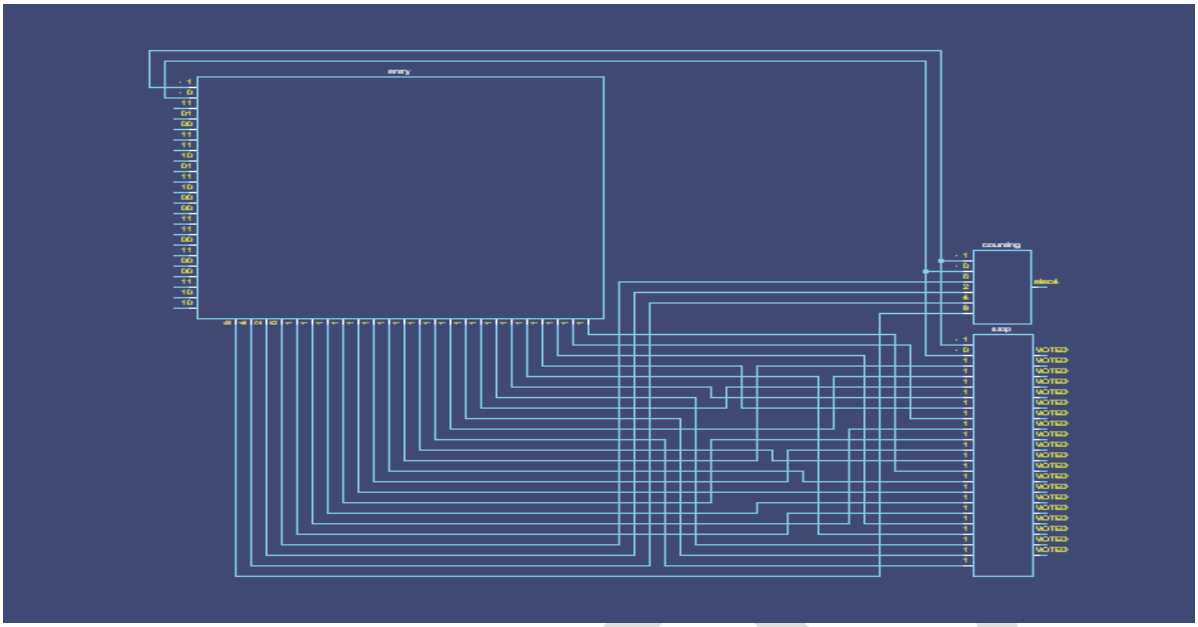

Fig 7: The overall logically connected blocks that drive commonly on the clear and clock signal.

CONCLUSION

The electronic voting machine using FPGA as the control unit has been implemented for faster verification of voter's eligibility in the polling booth and controlling multiple voting. The above simulated VHDL result can be burned and once the FPGA chip is made ready, ports can be assigned to all the software signals simulated and the hardware kit can be implemented using the Spartan 3E kit along with a female connecter. The major advantage of such mechanism is for eliminating multiple voting by the same voter automatically without much human intervention. The scope on such simulation lies in the effective method to identify each voter uniquely either through voter's identity or by biometric verification or even by family cards eligibility given to adults in it so that same voter is restricted from multiple voting or multiple identity.

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