A Microcontroller-Based Design for Digital Hearing Aid Devices

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ABSTRACT

Microcontrollers are emerging into new applications like smart phones, audio accessories, video gaming peripherals and advanced medical devices, providing high-performance, reliability and low-power consumption for end users. In this paper the design of a microcontroller-based hearing aid device is provided, by which power consumption and hardware area are reduced. The proposed digital hearing aid design comprises the following main components: sound detection circuit, microcontroller, digital to analog converter (DAC) and audio level indicator. The microcontroller used in this work is the high performance enhanced flash PIC18F4520 of microchip which has an on chip analog to digital converter (ADC) peripheral. The ADC features of PIC are used to detect and compare the sound level. 'C' and assembly language programs are developed to control the function of the microcontroller. MPLAB Integrated Development Environment (IDE) is applied for the development of the proposed embedded applications employing PIC microcontroller. The DAC MCP4921 is used for analog conversion of the processed signal. The different levels of the audio signal are indicated on the audio level indicator LM3915 in terms of ten LEDs display.

Key words: PIC microcontrollers; MPLAB ; hearing aids; audio level indicator.

INTRODUCTION

The pace of technological change in electronics and computer-aided designs has been extremely rapid in the past few decades. The results of this remarkable transformation are innovative products for medical applications which have vastly improved the delivery and effectiveness of health care for patients. Examples for these products include portable medical devices like blood pressure- and glucose monitors, insulin pumps and hearing instruments (hearing aids) [1] . Portable medical devices in general are expected to meet the following requirements: ease of use, high reliability and low-power operation as well as affordable cost [2]. Trade-offs between high functionality, low power consumption of portable devices along with high-performance and long battery life poses a challenge for designers in semiconductor companies and suppliers. This work focuses on the challenge in designing hearing aid devices. Hearing aids attempt to be the only way for enhancing the quality of life for millions of people who are suffering from mild to severe hearing loss. The introduction of digital signal processing into hearing aids has improved several features of traditional hearing aids such as fidelity and flexibility, as well as performance in noise, and restoration of functions for a variety of perplexing auditory deficits. Kruger

and Kruger have proposed that the late 1990's is known as the "period of the digital hearing aid"[3]. Figure 1 shows the basic architecture for a digital hearing aid [4].

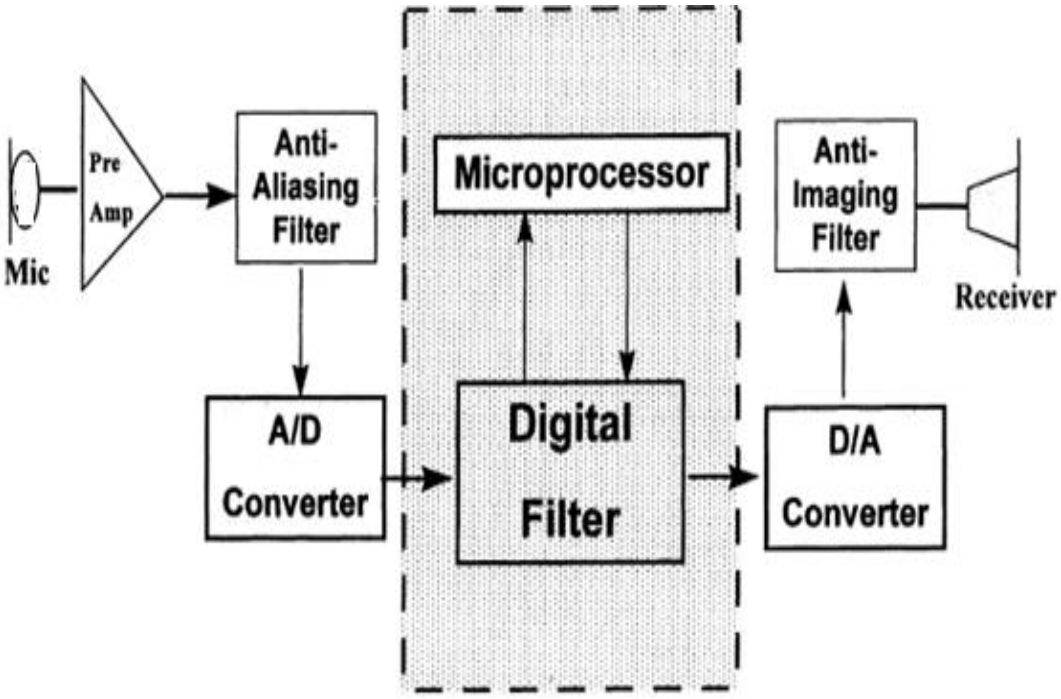

Fig1: Basic architecture of digital hearing aids

The architecture includes ADC and DAC to transform the signal into either digital or analog states. The anti-aliasing and anti-imaging filters serve to reduce distortions. Furthermore, digital devices can be programmed with multiple programs that can be invoked by the wearer, or that operate automatically and adaptively. These programs reduce acoustic feedback (whistling) or background noise, detect and automatically accommodate different listening environments (loud vs. soft, speech vs. music, quiet vs. noisy, etc.). For the recent years the designers have been working on reducing system cost by limiting the number of discrete components within the design and supplying highly integrated embedded control solutions that enable increased performance and reliability keeping power and cost constrains [5]. The technology of System on Programmable Chip (SOPC) and applying embedded soft-processor cores are employed for the design of digital hearing devices. In [6, 7] digital signal processing (DSP) modules are implemented on FPGA chips. In recent research work the application of the microcontroller units (MCU) on board has emerged as an alternative solution to the standard circuit design. Microcontrollers are especially designed to deliver high processing performance at the lowest supply currents of the entire electronic system as they support features like field-programmable non-volatile memory (in-system programmable flash memory) storage and flexible I/O configurations. Low-power microcontroller-based architectures for use in cochlear implants are described in [8]. Another sophisticated, low-power consumption, smart hearing aid was designed using microcontroller is given in [9]. That developed system saves battery power by switching on the sound amplifier section only when sound is detected. In this work a design of portable digital hearing aids is implemented employing the modern Peripheral Interface Controller PIC18F675 microcontroller of microchip. The proposed design focuses on reducing hardware area and power consumption

making use of the special features of PIC 18 such as having an internal comparator and ADC on chip which saves the need for external DAC. Furthermore, the complete system can be run on the internal frequency of the PIC. The function of the complete system is controlled by 'C' and assembly language programs developed and run on MPLAB Integrated Development Environment. The proposed design is compared with previous work illustrated in [9, 10] to assess its superiority.
This paper is organized as follows, in Section II design considerations with hearing aids is reviewed, the proposed system design is given section III, microcontroller based architecture is described in section IV, and finally conclusions are given in section V.

DESIGN CONSIDERATIONS WITH HEARING AIDS

The target of the audiologist in order to achieve the highest benefit and satisfaction of hearing aid technology is summarized in [11] as following:

a) improving audibility

b) maximizing comfort of soft and average sounds,

c) maximizing comfort and speech intelligibility in noise,

d) keeping loud sounds within range of comfort.

The majority of patients using hearing aids have sensorineural hearing loss causing an inability to perceive low-intensity sounds. In this case the amplifiers used in hearing aids provide more gain for soft sounds relative to average and loud sounds. Recently, wide dynamic range compression (WDRC) is the accepted amplification strategy, allowing the hearing aid to fit sound into the residual dynamic range of the patient. WDRC applies compression kneepoints less than 60dB sound pressure level (SPL) and low compression ratios lower than 4:1 to keep as much of the audio signal as possible into the residual dynamic range of the patient. Audibility of the speech signal is restored based on frequency-dependent amplification. This is achieved by providing high amplification gain across the range of frequencies wherein a hearing loss is present. It is the job of the audiologist to decide the gain required at each frequency. One of the approaches used for adults is a loudness equalization procedure, which makes amplified sound equally loud across the frequency spectrum in order to maximize intelligibility. Loudness equalization fitting formulas take both audibility and comfort into account. Digital hearing aids can be programmed to frequency-dependent amplification to provide good sound quality. On the other hand, loudness normalization fitting formulas deliver amplified sounds to the end-user at a loudness level equal to that of a normal-hearing listener. After hearing thresholds of the patient have been measured, these values can be entered into the fitting software chosen to generate a prescriptive fitting target.

SYSTEM DESIGN

The block diagram of the proposed system is shown in Fig. 2. The building blocks are: sound detection circuit, signal processing core which employs a microcontroller chip, DAC; audio level indicator and earphone.

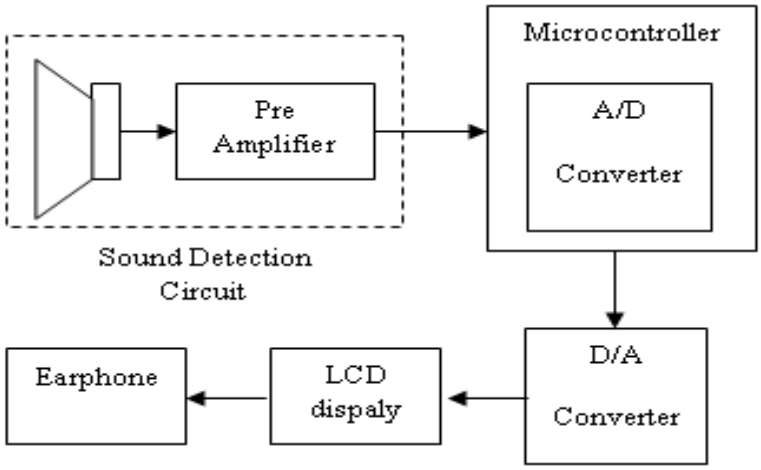

Fig 2: Block diagram of the hearing aids device.

The features of the distinct building blocks are explained in the following.

A. Sound Detection Circuit

The microphone, amplifier along with resistors and capacitors build the sound detection circuit [12]. A typical sound detection circuit is shown in Fig.3. The directional microphone is applied here because it has the benefit of amplifying sounds which are facing the listener more than sounds or noise from behind or other directions. This feature makes a directional microphone provide an acceptable signal to noise ratio and improves speech understanding in noise.

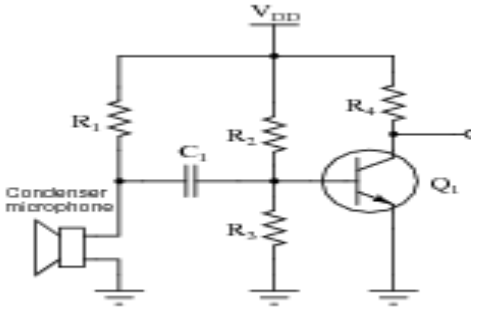

Fig 3: Sound detection circuit.

B. Microcontroller Unit

In this work the powerful PIC18F4520 8-bit microcontroller of microchip is used. It is specially chosen because it has several features making it ideal for advanced level analog to digital applications in automotive, medical and consumer applications. The instruction set of PIC 18 consists of 35 single word instructions with three general formats for the instructions. All instructions are single cycle except for program branches or jumps. Some of the features are mentioned in the following table. More about PIC microcontroller is found in [13].

Table1. Features of PIC microcontroller

CPU and memory	CPU speed OF 10 MIPS C compiler optimized RISC architecture 32 k Bytes Flash Program Memory 1,536 Byte RAM Data Memory 256 Byte EEPROM Data Memory
System	Internal oscillator support-31 kHz to 8MHz with 4xPLL Fail-Safe Clock Monitor Watchdog Timer with separate RC oscillator
Power Managed Modes	Run, Idle and SLEEP modes Idle mode for currents of typical values down to 5.8uA Sleep mode for currents of typical values to 0.1uA
Analog Features	10-bit ADC, 13 channels, 100K samples per second Two Analog Comparators multiplexing
Peripherals	Master Synchronous Serial Port supports master and slave mode EUSART module including LIN bus support Four Timer modules 5 PWM outputs 2 Capture / Compare
Special Microcontroller Features	100,000 erase/write cycle Enhanced FLASH program memory typical 1,000,000 erase/write cycle Data EEPROM memory FLASH/Data EEPROM Retention: > 40 years Self-reprogrammable under software control Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST) Programmable code protection Power saving SLEEP mode In-Circuit Debug (ICD) via two pins
CMOS Technology	Low power, high speed FLASH/EEPROM technologyFully static design Wide operating voltage range (2.0V to 5.5V) Industrial and Extended temperature ranges

C. The Digital to Analog Converter

The DAC MCP4921 applied in this work belongs to the Microchip Technology Inc. MCP492X. MCP492X are 2.7 –5.5V, low-power 12-Bit DACs with Serial Peripheral Interface **(**SPI) which provides high accuracy and low noise performance for applications where calibration or compensation of signals is required. SPI is a standard for controlling almost any digital electronics that accepts a clocked serial stream of bits. MCP4921 is an easy-to- program and configure DAC as it only accepts a 2 byte instruction of which 12 bits is the data and the 4 most significant bits are used to control the device. More about MCP4921 is found in [13].

D. Audio Level Indicator

LM3915 from National Semiconductor used here is a monolithic integrated circuit which displays the audio sound level in terms of ten LEDs and provides a logarithmic 3 dB/step analog display.

MICROCONTROLLER BASED ARCHITECTURE

According to [13] there are seven important non I/O pins of PIC. First is the MCLR (master clear) pin, which is active low. A switch is connected from that pin to ground to reset PIC when necessary. Biasing are Vdd (pin 11 and 32) and Vss (pin 12, 31). An oscillator is connected across pin 13 and 14 to provide external clock to provide the timing signals necessary for program execution. The remaining 33 pin are configured as I/O pin. The analog signal received from the microphone and board amplifier is interfaced with the ADC peripheral of the PIC microcontroller where it is converted to a digital outputs. The ADC module on the PIC has four special function registers associated with it:

1) Result High Register (high byte) ADRESH ,
2) Result Low Register (low byte) ADRESL to store the output from the converter
3) Control Register 0 (ADCON0)
4) Control Register 1 (ADCON1

The ADCONO register is used to set the conversion time and select the analog input channel. The ADON bit is used to turn on the ADC else the ADC is turned off when the microcontroller is powered up to reduce power consumption. ADCS1 and ADCS0 set the conversion time. The GO_DONE bit is used to check if the conversion is finished. Setting this bit initiates the start of conversion then the bit is cleared when the conversion is complete. CHS2, CHS1 and CHS0 are the channel select bits to determine which input pin is routed to the ADC. ADCON1 is split into two sections. The first section is a single bit, the result format selection bit ADFM which selects if the output is right justified (bit set) or left justified (bit cleared). The advantage is the possibility to use as an 8 bit converter (instead of ten bit) by clearing this bit, and reading just ADRESH and ignoring the two least significant bits in ADRESL. The second section includes the A/D port configuration control bits PCFG3-0 . The default of PCFG = 0000 makes the 8 pins RA0-RA3 and RA5 as well as RE0-RE2 used for analog inputs. The internal RC oscillator is used for the conversion clock

source. In this case the conversion time per bit T_{ad} is typically 4-6µs and the conversion time ($12 \times T_{ad}$) = 72 µs. The converted data is then sent to the DAC to replicate the signal. The PIC is interfaced with SPI DAC MCP4921. The benefit of using a SPI DAC is that only 3 microcontroller pins are required instead of 10-12 pins as in conventional parallel DAC. As MCP4921 is a 12-bit DAC whereas PIC is an 8-bit microcontroller, the 8 bit output of PIC is converted into a 12 bit output. This output is now fed into the audio level indicator, LM3915, to indicate the level of the audio signal at the ear phone. The flowchart describing the whole process is given in Fig.4. The complete circuit diagram is shown in Fig 5. The features of the proposed design are reduced hardware area and circuit complexity compared to the design given in [10], which applies an external ADC.

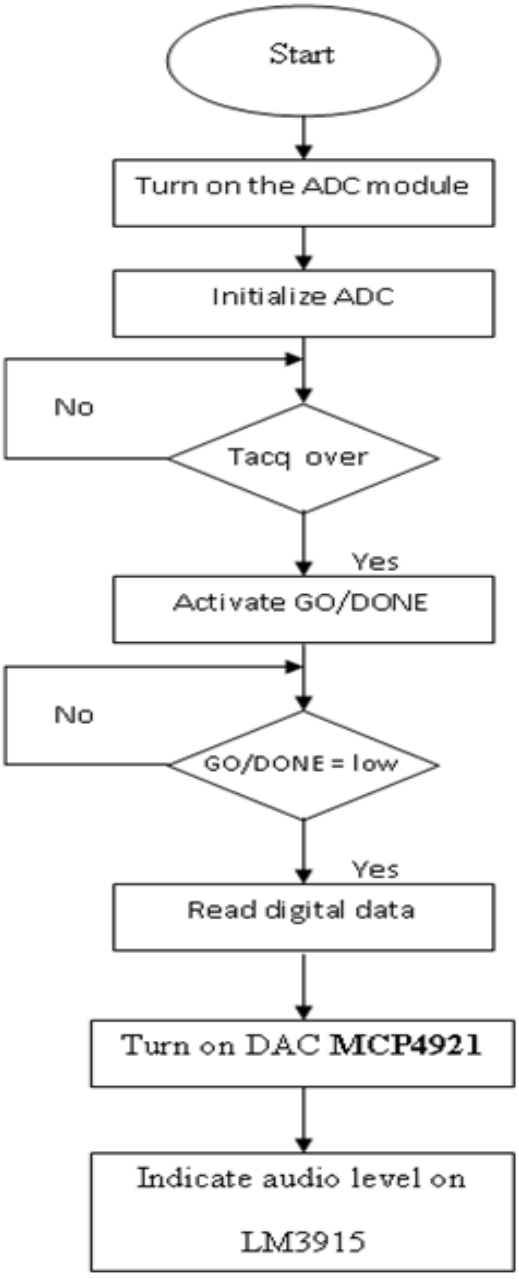

Fig4. Flowchart of the processing program.

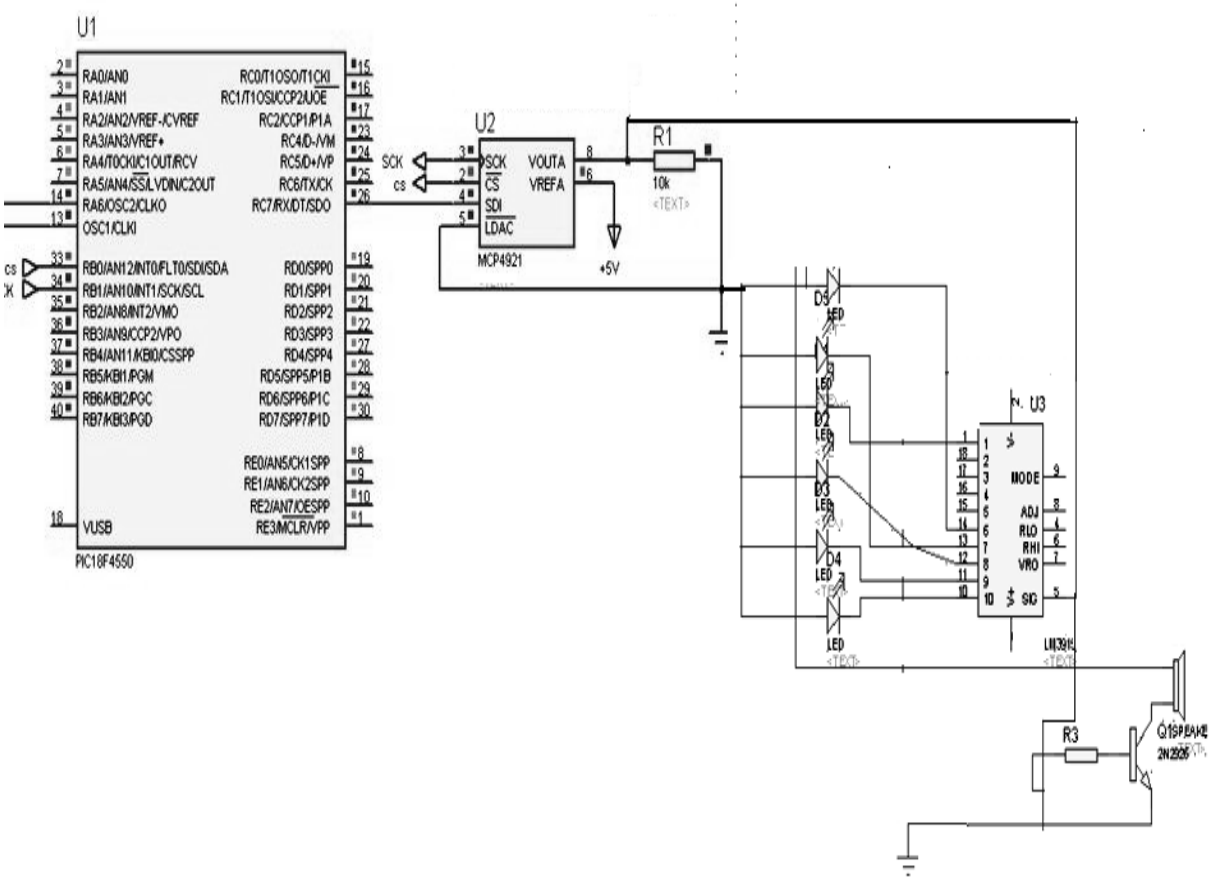

Fig5: The complete circuit diagram of the hearing aids device.

CONCLUSION

In this work a microcontroller based low-power hearing aid was implemented. The microcontroller used is the powerful Flash PIC18F675. The advantage of PIC 18 is having an internal comparator and ADC on chip which reduces complexity of design. Furthermore, the complete system can be run on the internal frequency of the PIC which saves the need for external oscillator circuits. The function of the complete system is controlled by C and assembly language programs developed and run on MPLAB Integrated Development Environment. The proposed hearing aid is comparable and superior to designs in previous research work. This is achieved through the increased integration of components, which perform separate targets and are then interconnected to work as a complete system.

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