A Configurable Linear Feedback Shift Register (LFSR) 

For Low power built in Self-Test

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Abstract

As the technology is growing on we need to design a system that provides low power consumption and high speed and should be area efficient, among these power is a major constraint here, a new algorithm proposed it is based on low transition test pattern generator using a linear feedback shift register (LFSR) called LT-LFSR reduce the average and peak power of a circuit during test by generating three intermediate patterns between the random patterns. The goal of having intermediate patterns is to reduce the transitional activities of Primary Inputs (PI) which eventually reduces the switching activities inside the Circuit under Test (CUT) and hence, power consumption. The random nature of the test patterns is kept intact. The area overhead of the additional components to the LFSR is negligible compared to the large circuit sizes. The experimental results for ISCAS’85 and ’89 benchmarks, confirm up to 77% and 49% reduction in average and peak power, respectively.

Keywords- CUT, Optimization, Primary inputs (PI), Test Pattern Generation, BIST, and LFSR

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. The applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. Hence the important aspect to optimize power during testing.

The power dissipation in CMOS technology is either static or dynamic. Static power dissipation is primarily due to the leakage currents and contribution to the total power dissipation is very small. The dominant factor in the power dissipation is the dynamic power which is consumed when the circuit nodes switch from 0 to 1. During switching, the power is consumed due to the short circuit current flow and the charging of load capacitances is given by equation:

\[ P = \frac{1}{2} V_{DD}^2 E(\text{sw}) C_L F_{CLK} \]
Where $V_{DD}$ is supply voltage, $E_{(sw)}$ is the average number of output transitions per $1/F_{CLK}$, $F_{CLK}$ is the clock frequency and $C_L$ is the physical capacitance at the output of the gate. Dynamic power dissipation contributed to total power dissipation. From the equation dynamic power depends on three parameters: supply voltage, clock frequency and switching activity.

The power dissipation of a system in test mode is more than in normal mode. Low correlation between consecutive test vectors (e.g. among pseudorandom patterns) increases switching activity and eventually power dissipation in the circuit. The extra power (average or peak) can cause problems such as instantaneous power surge causes circuit damage, formation of hot spots, difficulty in performance verification and reduction of the product yield and life time.

Automatic test equipment (ATE) is the instrumentation used in external testing to apply test patterns to the CUT, to analyze the responses from the CUT, and to mark the CUT as good or bad according to the analyzed responses. External testing using ATE has a serious disadvantage, since the ATE (control unit and memory) is extremely expensive and cost is expected to grow in the future as the number of chip pins increases. As the complexity of modern chips increases, external testing with ATE becomes extremely expensive. Instead, Built-In Self-Test (BIST) is becoming more common in the testing of digital VLSI circuits since overcomes the problems of external testing using ATE. BIST test patterns are not generated externally as in case of ATE.

II. LOW POWER TESTING SCHEMES

Various authors reported on techniques to cope with power problems during testing. Existing low-power testing scheme is divided into the following two categories.

(A) Low - Power Testing Techniques for Internal Testing

(B) Low - Power Testing Techniques for External Testing

B. Low-Power Testing Techniques for Internal Testing

The technique proposed in consists of a distributed BIST control scheme that simplifies BIST architecture for complex ICs, especially during higher levels of test activity. The approach can schedule the execution of every BIST element to keep the power dissipation under specified limits. The technique reduces average power and avoids temperature-related problems but increase in test time. A BIST strategy called dual-speed LFSR is proposed in to reduce the circuit’s overall switching activities.

The technique uses two different-speed LFSRs to control those inputs that have elevated transition densities. The low power test pattern generator presented in is based on cellular automata, reduces the test power in combinational circuits while attaining high fault coverage. Test time and area overhead remain unaffected. Another low-power test pattern generator based on a modified LFSR is proposed in . The scheme reduces the power in CUT in general and clock tree in particular.

Gizopoulos et al. consider the problem of low-power BIST for data path architecture built around multiplier-accumulator pairs. The method proposes two alternative architectures depend on low energy or low power dissipationThe drawback of these techniques is circuit-dependent, implying that non-detecting subsequences must be determined for each circuit test.
sequence. Other authors propose two other low-power approaches for scan-based BIST. Zhang, Roy, and Bhawmik propose modifying the LFSR by adding weight sets to tune the pseudorandom vector’s signal probabilities and thereby decrease energy consumption and increase fault coverage.

A low-power random pattern generation technique to reduce signal activities in the scan chain is proposed in . In this technique, an LFSR generates equally probable random patterns. The technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power. Girard et al. address the problem of energy minimization during test application for BIST enabled circuits. is a more important parameter. Therefore, the authors propose a method based on a simulated-annealing algorithm to select an LFSR’s seed and provide the lowest energy consumption. Test vector inhibiting techniques to filter out some non-detecting subsequences of a pseudorandom test set generated by an LFSR.

A. Low-Power Testing Techniques for External Testing

The category contains various techniques adopted to reduce the power consumption during external testing by ATE and depends on the number of transitions in test data set. Presents a low capture power ATPG and a power-aware test compaction method. This ATPG lowers the growth of test pattern count compared to the detection number. The peak power becomes smaller as the detection number increases. The test compaction algorithm further reduces the number of test patterns as well as the average capture power.

The idea is to identify an input control pattern such that, by applying that pattern to the primary inputs of the circuit during the scan operation, the switching activity in the combinational part can be minimized or even eliminated. The basic idea of input control technique with existing vector- or latch-ordering techniques that reduces the power consumption has been covered in . In the same area, The researchers have widely explored the test vector reordering techniques to reduce the switching power. Hamming distance based reordering is described in survey paper Sankaralingam et al. Vector compaction and data compression based on a static compaction technique to minimize the scan vector power dissipation. Carefully selecting the merging order of test cube pairs during static compaction reduces both average and peak power for the final test set. The technique is more effective than conventional static compaction techniques that randomly merge test cubes. Chandra and Chakrabarty propose a novel technique using test data compression for testing that reduces both test data volume and scan power dissipation.

III. PATTERN GENERATOR

The BIST contains two major components: test pattern generator and response checker. Both of these components use Linear Feedback Shift Register (LFSR). The paper described the three different pattern generation techniques by using LFSR can be designed to reduce the power consumption during test in the following ways.

A. Generating Test Vectors by using Modified Clock Scheme.

The low-power test pattern generator (TPG) based on modified clock scheme. The low-power BIST technique relies on a gated clock scheme for the pseudo-random test pattern generator and the clock tree feeding the TPG. An n-bit LFSR is divided into two n/2-bit LFSRs. Basically; a clock whose speed is half of the normal speed is used to activate one half of the D flip-flops in the TPG (i.e. a modified LFSR) during one clock cycle.

During the next clock cycle, the second half of the D flip-flops is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with a
master clock CLK and have the same but shifted in time period.

The clock CLK is the clock of the circuit in the normal mode and has a period equal to T. As one can observe, a test vector is applied to the CUT at each clock cycle of the test session, only one half of the circuit inputs can be activated during the time.

Another important feature is the total energy consumption during BIST is reduced, since the test length produced by the modified LFSR is roughly the same than the produced by a conventional LFSR to reach the same or sometimes a better fault coverage.

B. Generating Test Vectors by using LT-LFSR

Mohammad Tehran poor proposed a low-transition LFSR by combining techniques of random pattern generation called R-Injection (RI) and Bipartite LFSR for low-power BIST. The new LT-LFSR generates three intermediate patterns. The RI method inserts a new intermediate pattern between two consecutive test patterns by positioning a random-bit (R) in the corresponding bit of the intermediate pattern when there is a transition between corresponding bits of pattern pairs.

The bipartite LFSR generates an intermediate pattern using one half of each of the two consecutive random patterns. The goal is to design a new random pattern generator reduces the total number of transitions among the adjacent bits in each random pattern (horizontal dimension) and transitions between two consecutive random patterns (vertical dimension) as well. In other words, the new low transition random pattern generator increases the correlation between and within patterns.

The main advantage of the technique can be used for both combinational and sequential circuits and the randomness quality of patterns does not deteriorate. The authors also use a k-input AND gate and T-latch to generate a high correlation between neighboring bits in the scan chain, reducing the number of transitions and the average power.

C. Generating Test Vectors by using LPATPG

Zhang.X proposed a Low Power Automatic Test Pattern Generator (LPATPG) with peak power reduction. The authors used two n-bit random pattern generators and n (2 x 1) multiplexers but only add one flip flop to an n-bit LFSR, therefore the area overhead of bipartite LFSR is much lower than LPATPG.

IV. BIST ARCHITECTURE

BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external ATE

A. Implementation of BIST

A typical BIST architecture consists of Test Pattern Generator (TPG) usually implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register (MISR), CUT and BIST control unit as shown in figure 1.

TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically
CUT: It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (PO) delimit it.

BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs.

MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures with every small probability of alias.

TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not.

B. Implementation of low transition test pattern

The technique proposes a new transition test pattern generation technique which generates three intermediate test patterns between each two consecutive random patterns generated by a conventional LFSR. The proposed test pattern generation method does not decrease the random nature of the test patterns. The technique reduces the PI’s activities and eventually switching activities in the circuit under test. Let us assume that $T^i$ and $T^{i+1}$ are two consecutive test patterns generated by a pseudorandom pattern generator (e.g. a conventional LFSR). The new low transition LFSR (LT-LFSR) generates three intermediate patterns ($T^{i1}$, $T^{i2}$ and $T^{i3}$) between $T^i$ and $T^{i+1}$. 
C. Implementing algorithm for LT-LFSR

The proposed approach consists of two half circuits. The algorithm steps says the functions of both half circuits is

Step1: First half is active and second half is idle and gives out is previous, the generating test vector is \( T^1 \).

Step2: Both halves are idle First half sent to the output and second half’s output is sent by the injection circuit, the generating test vector is \( T^{i1} \).

Step3: Second half is active First half is in idle mode and gives out as previous, the generating test vector is \( T^{i2} \). Step4: Both halves are in idle mode, First half is given by injection circuit and Second half is same as previous, the generating test vector is \( T^{i3} \). After completing step 4 again goes to step1 for generating test vector \( T^{i+1} \).

V. RESULTS:

The proposed approach is a new low power pattern generation technique is implemented using a modified conventional LFSR.

Comparisons of the number of test patterns (\( N_P \)) required to hit target fault coverage (FC), the average and peak power of LT-LFSR, LPATPG and modified clock scheme are shown in Table-1. The used 50 different seeds for 10 different polynomials in the experiment. The performance of LT-LFSR is seed and polynomial-independent. The required number of patterns provides target FC does not quadruples, and preserving randomness.

TABLE 1 COMPARISON OF FAULT COVERAGE NO OF TEST PATTERNS, AVERAGE AND PEAK POWER

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>c1908</th>
<th>S38417</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC%</td>
<td>95.9</td>
<td>95.3</td>
</tr>
<tr>
<td>( N_P )</td>
<td>863</td>
<td>1116</td>
</tr>
<tr>
<td>( \Delta P \text{ avg} )</td>
<td>75.5</td>
<td>32</td>
</tr>
<tr>
<td>( \Delta P \text{ peak} )</td>
<td>40.7</td>
<td>33</td>
</tr>
</tbody>
</table>

VI CONCLUSION

By using this low transition test pattern generator using LFSR for Test Pattern Generation (TPG) technique we conclude that power dissipation is reduced during testing. The transition is reduced by increasing the correlation between the successive bits, reduces the average and peak power of a circuit during the test mode. By increasing the correlation between the test patterns in the CUT and eventually the power consumption is reduced. Additional intermediate test patterns inserted between the
original random patterns reduces the PI activities, average and peak power of combinational and sequential circuits during the test mode with do not effect on FC.

REFERENCES