DESIGN AND ANALYSIS OF ADAIABATIC FULL SUBTRACTOR FOR LOW POWER APPLICATIONS

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ABSTRACT

The power consumption of the electronic devices can be reduced by adopting different design styles. Adiabatic logic style is said to be an attractive solution for such low power electronic applications. This paper presents an energy efficient technique for digital circuits that uses adiabatic logic. The proposed technique has less power dissipation when compared to the conventional CMOS design style. This paper evaluates the basic full subtractor in different adiabatic logic styles and their results were compared with the conventional CMOS design. The simulation results indicate that the proposed technique is advantageous in many of the low power digital applications.

Key words: Low power, charge recovery, sinusoidal power clock, complimentary, alternating current.

INTRODUCTION

From the past few decades CMOS technology plays a dominant role in designing low power consuming devices. Compared to different logic families CMOS has less power dissipation which made it superior over the previous low power techniques. The power consumption in conventional CMOS circuit is due to switching activity of the devices from one state to another state and due to the charging and discharging of load capacitor at the output node. The power dissipation in conventional CMOS design can be minimized by reducing the supply voltage, node capacitance value and switching activity. But reducing the values of these parameters may degrade the performance of the device. So an efficient low power technique other than CMOS is needed that has less power dissipation compared to CMOS which can be done by using adiabatic technique.

The present paper focuses on a novel energy efficient technique called adiabatic logic which is based on energy recovery principle. In this technique instead of discharging the consumed energy is recycled back to the power supply thereby reducing overall power consumption. In the present paper the performance of full subtractor is evaluated in different adiabatic logic styles and their results were compared with the conventional CMOS design. As arithmetic circuits are the basic building blocks of many of the digital circuits, the present paper mainly concern on its design. The performance of this full subtractor was evaluated in different adiabatic techniques of ECRL, PFAL, 2PASCL, and PFAL&2PASCL. Simulation results shows that the proposed technique is efficient over the conventional CMOS design in terms of power dissipation.

CMOS DESIGN

CMOS is the basic building block of many of the digital circuits. The CMOS circuit itself acts as an inverter. It can be realized as a combination of PMOS in the pull up section whose source is connected to power supply and NMOS in the pull down section whose source is connected to ground and the output is taken across the drain junction of the two devices. The CMOS circuit has less power dissipation when compared to many of the previous VLSI families of RTL, TTL and ECL. The power consumption in CMOS is due to the switching activity of the transistors from one state to another state, charging and discharging of the load capacitance and frequency of operation.

(i) INVERTER

The basic CMOS inverter circuit is shown in figure 1.

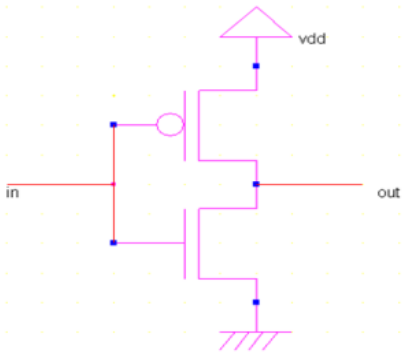

Fig. 1: CMOS inverter

The operation of the circuit can be evaluated in two stages of charging phase and discharging phase. During the charging phase, the input to the circuit is logic LOW. During this phase, the PMOS transistor conducts and NMOS transistor goes in to OFF state which charges the output value to power supply results in logic HIGH output. The equivalent circuit consists of a resistor in series with the output load capacitance which shows a charging path from power supply to output terminal. Here the resistor acts ac PMOS ON resistor.

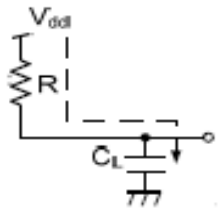

Fig. 2: Equivalent circuit for charging process in CMOS

During the discharging phase, the input to the circuit is logic HIGH. During this phase, the NMOS transistor conducts and PMOS transistor goes into OFF state which results in a discharging path from output terminal to ground. The value that is stored at the output during the charging phase discharges towards the ground results in logic LOW output. The equivalent circuit consists of a resistor in series with output terminal to ground. Here the resistor acts as NMOS ON resistor.

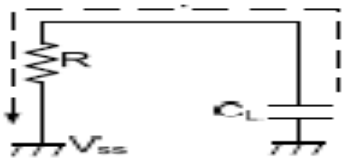

Fig. 3: Equivalent circuit for discharging process in CMOS

From the operation of the CMOS design it is evident that during the charging process, the output load capacitor is charged to $Q = C_L V_{dd}$ and the energy stored at the output is $(½)C_L V_{dd}^{2.}$ During the discharging phase, the amount of energy dissipated is also $(½)C_L V_{dd}^2$. So the total amount of energy dissipated during the charging and discharging phases is

$$E_{dissipated} = C_L V_{dd}^2 \qquad (1)$$

The power consumption of the CMOS circuit is based on the following equation

$$P = CV^2 f \qquad (2)$$

From the equation it is evident that the power dissipation of CMOS can be reduced by minimizing the supply voltage, node capacitance and switching activity to some extent. But reducing the values of these parameters may suffer from some disadvantages. Reducing the load capacitance is strongly limited by the technology. Reducing the supply voltage may degrade the performance of the device. Reducing the supply voltage may also suffer from leakage problems. In order to overcome these problems an efficient low power technique called adiabatic logic is explained in this paper.

(ii) Full Subtractor

Arithmetic circuits are the most important elements in the design of many VLSI digitl circuits. We must design chips in such a way that it must consume less power and dissipation less power with efficient output. Full subtractor is one of the arithmetic circuits which is widely used in internal chip design of many digital circuits. It has three inputs and two outputs which are difference and borrow.

Table 1: Truth table of Full Subtractor

A	B	C	DIFF	BORR
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 1 shows the truth table for full subtractor with three inputs and two outputs of difference (DIFF) and borrow (BORR).

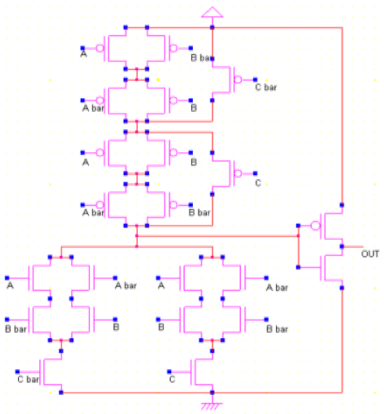

Fig. 4: Circuit for CMOS Difference

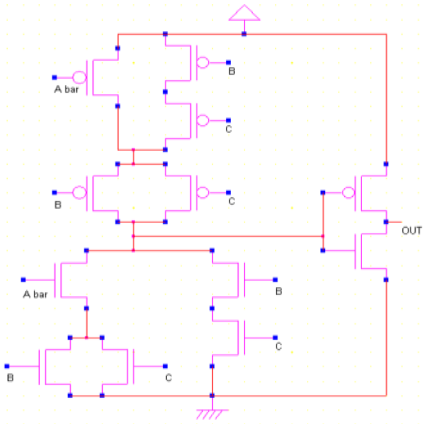

Fig. 5: Circuit for CMOS Borrow

ADIABATIC LOGIC

Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as “energy recovery” or “charge recovery” logic. As the name itself indicates that instead of dissipating the stored energy during charging process at the output node towards ground it recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases. The adiabatic logic uses AC power supply instead of constant DC supply, this is one of the main reasons in the reduction of power dissipation.The adiabatic logic can be explained with the help of basic inverter circuit

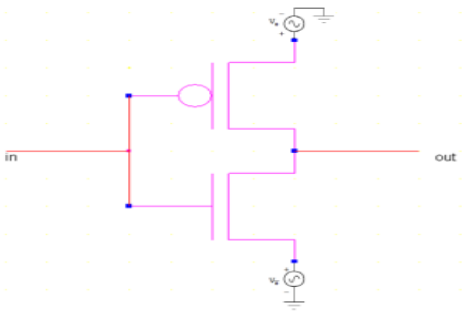

Fig. 6: Adiabatic inverter

The adiabatic inverter circuit can be constructed using CMOS inverter with two AC power supplies instead of DC supply. The power supply’s are arranged in such a way that one of the clock is in phase while the other is out of phase with the first one. The operation of the adiabatic inverter can be explained in two stages. During the charging phase, the PMOS transistor conducts and NMOS transistor goes into OFF state which charges the output load capacitor towards the power supply results in logic HIGH output.

Fig. 7: Equivalent circuit for charging process in adiabatic inverter

During discharging phase, the NMOS transistor conducts and PMOS transistor goes into OFF state. Instead of discharging the stored value at the output towards ground, the energy is recycled back to the power supply. Its equivalent circuit consists of a resistor in series with output load capacitance and power supply.

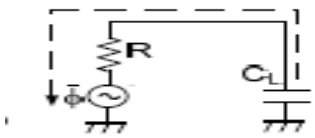

Fig. 8: Equivalent circuit for charge recovery process in adiabatic inverter

The charging process and the charge recovery process are efficient only when the charging voltage is varying one. Lower the rate of charging, lesser the power drawn from the supply voltage.

ADIABATIC TECHNIQUES

Adiabatic logic has a different logic style which helps in the reduction of the power dissipation of the circuit. The present paper explains basic universal gates using some of the important adiabatic techniques.

(i) ECRL

Efficient charge recovery logic consists of two cross couple PMOS transistors in the pull up section where as the pull down section is constructed with a tree of NMOS transistors. Its structure is similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. The logic function in the functional block can be realized with only NMOS transistors in the pull down section. The basic full subtractor in ECRL logic can be constructed as

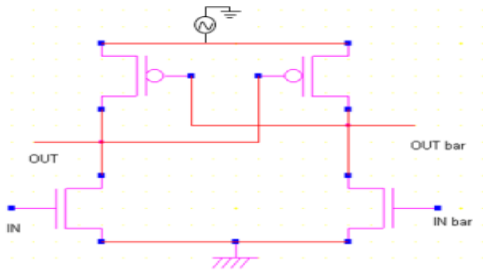

Fig. 9: ECRL inverter

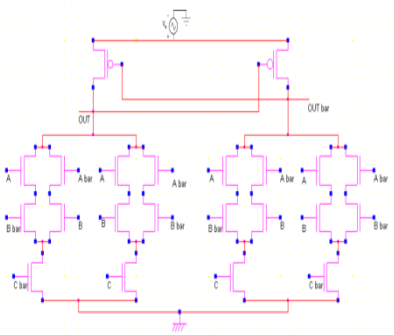

Fig. 10: ECRL Difference

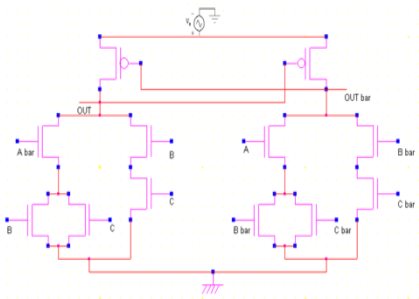

Fig. 11: ECRL Borrow

(ii) PFAL

The Positive Feedback Adiabatic Logic is a partial energy recovery circuit. It is also known as PAL-2N (Pass transistor Adiabatic Logic). The core of PFAL logic is a latch made up of two PMOS and two NMOS transistors that avoid logic level degradation on the output nodes. The logic function in the functional block can be realized with only NMOS transistors connected parallel to the PMOS transistors. The primary advantage of PFAL over ECRL is that the functional blocks are in parallel with the PMOSFETs forming transmission gate. It also has the advantage of implementing both the true function and its complimentary function.

Using PFAL, the basic universal gates can be constructed as

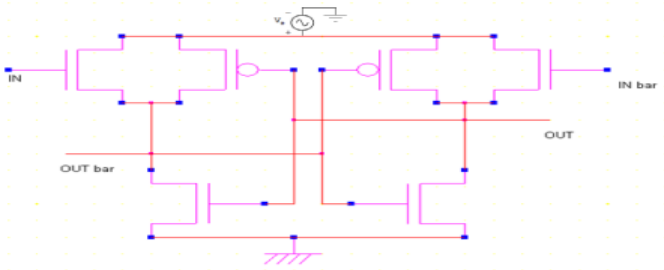

Fig. 12: PFAL inverter

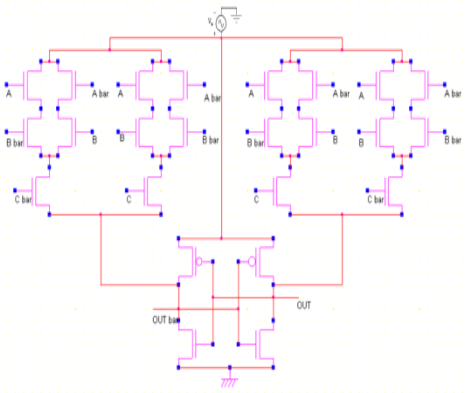

Fig. 13: PFAL Difference

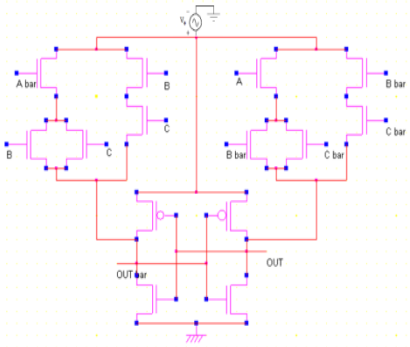

Fig. 14: PFAL Borrow

(iii) 2PASCL

The Two Phase Adiabatic Static Clocked Logic (2PASCL) uses two phase clocking split level sinusoidal power supply's which has symmetrical and unsymmetrical power clocks where one clock is in phase while the other is out of phase. The circuit has two diodes in its construction where one diode is placed between the output node and power clock, and another diode connected between one of the terminals of NMOS and power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. The circuit operation is divided into two phases "hold phase" and "evaluation phase". During the evaluation phase, the power clock swings up and power source swings down. During the hold phase, the power source swings up and power clock swings down.

Using 2PASCL the basic universal gates can be constructed as

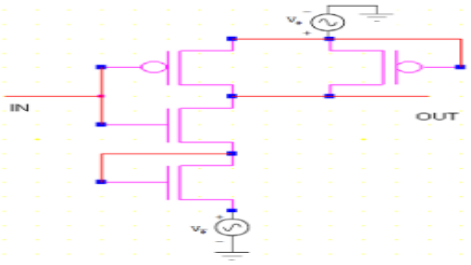

Fig. 15: 2PASCL inverter

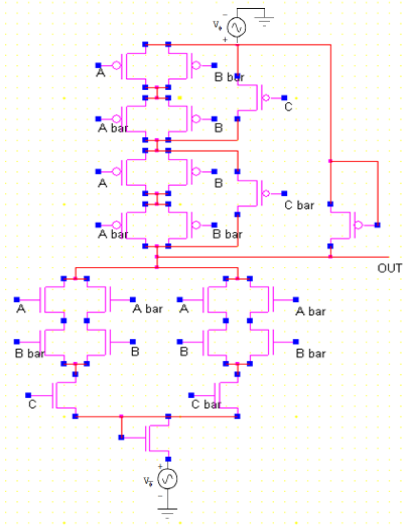

Fig. 16: 2PASCL Difference

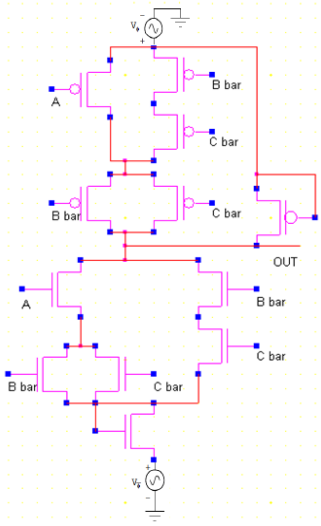

Fig. 17: 2PASCL Borrow

(iv) PFAL& 2PASCL

The PFAl&2PASCL logic can be realized as a combination of both PFAL and 2PASCL. Its structure is similar to 2PASCL except the core part of 2PASCL is replaced by PFAL logic circuit. It has two power clock signals operated in two different modes. The major advantage of this technique is it has less power dissipation compared to ECRL and PFAL and it also gives the true function and complementary function of a given circuit.

Using PFAL&2PASCL, the basic universal gates can be constructed as

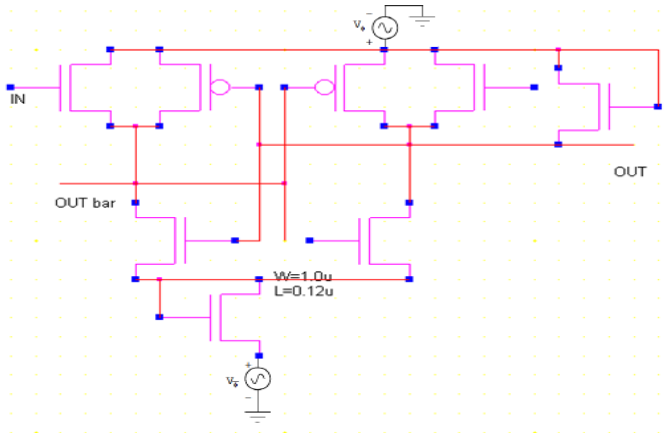

Fig. 18: PFAL&2PASCL inverter

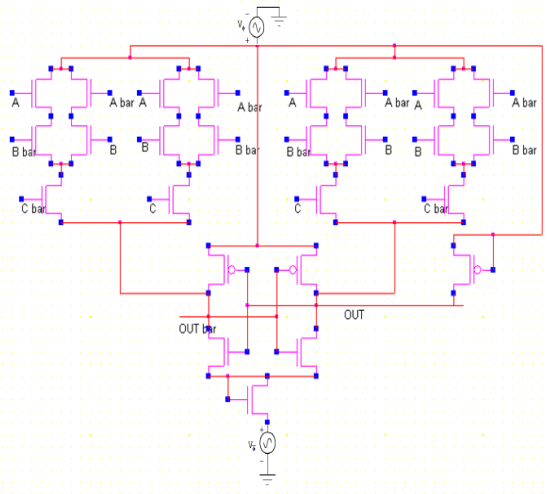

Fig. 19: PFAL&2PASCL Difference

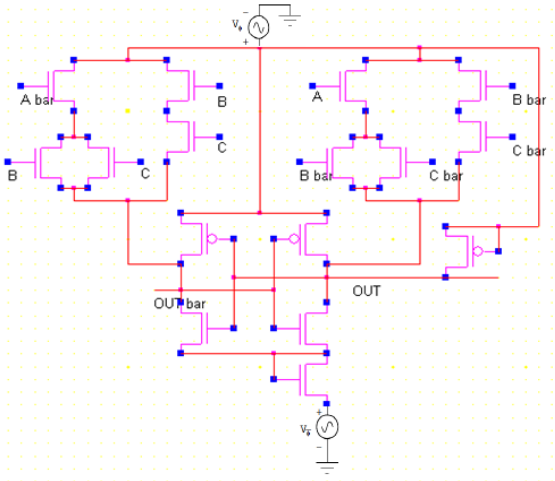

Fig. 20: PFAL&2PASCL Borrow

SIMULATION RESULTS AND DISCUSSION

The simulation results were verified using PSPICE software. The simulation results of full subtractor in conventional CMOS design and different adiabatic logic design styles were presented in this section.

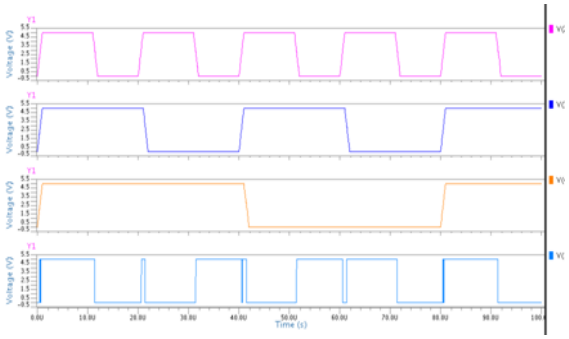

Fig. 21: Simulated waveforms of CMOS Difference

Fig. 21 shows the simulated waveforms of CMOS Difference, where the top three signals indicate inputs and the bottom signals indicates Difference.

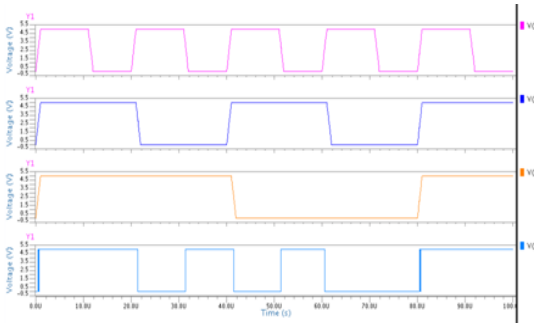

Fig. 22: Simulated waveforms of CMOS Borrow

Fig. 22 shows the simulated waveforms of CMOS Borrow, where the top three signals indicate inputs and the bottom signal indicates Borrow.

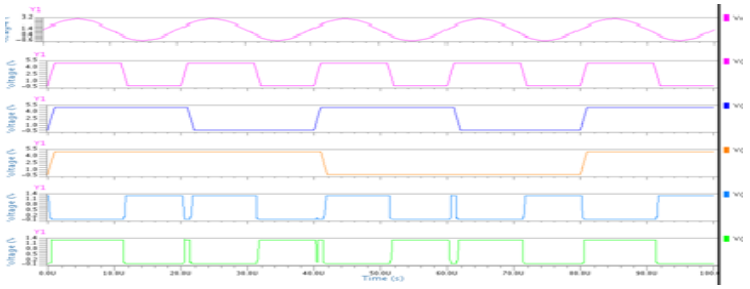

Fig. 23: Simulated waveforms of ECRL Difference

Fig. 23 shows the simulated waveforms of ECRL Difference, where the topmost signal indicates sinusoidal power clock, three signals below it are inputs and the bottom two signals indicate output bar and output signals respectively.

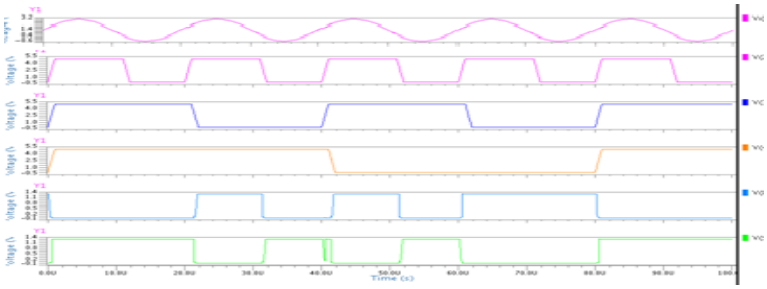

Fig. 24: Simulated Waveforms of ECRL Borrow.

Fig. 24 shows the simulated waveforms of ECRL Borrow, where the topmost signal indicates sinusoidal power clock, three signals below it are inputs and the bottom two signals indicate output bar and output signals respectively.

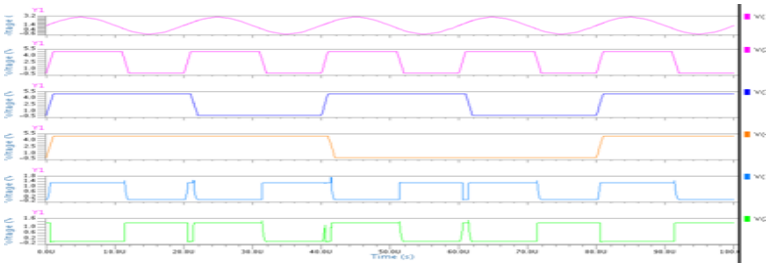

Fig. 25: Simulated Waveforms of PFAL Difference

Fig. 25 shows the simulated waveforms of PFAL Difference, where the topmost signal indicates sinusoidal power clock, three signals below it are inputs and the bottom two signals indicate output and its complimentary signals respectively.

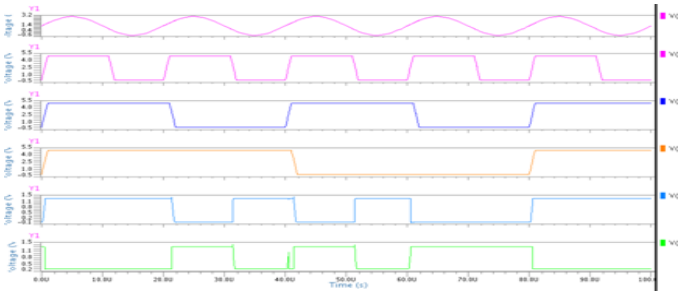

Fig. 26: Simulated Waveforms of PFAL Borrow

Fig. 26 shows the simulated waveforms of PFAL Borrow, where the topmost signal indicates sinusoidal power clock, three signals below it are inputs and the bottom two signals indicate output and its complimentary signals respectively.

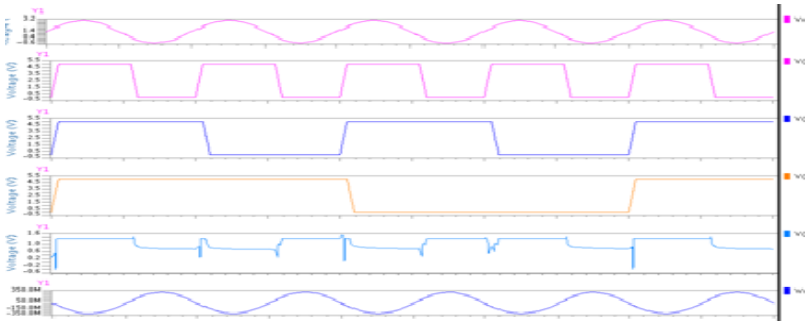

Fig. 27: Simulated Waveforms of 2PASCL Difference

Fig. 27 shows the simulated waveforms of 2PASCL Difference, where top and bottom signals are sinusoidal power clocks, the signals between them are three input signals and output signal respectively.

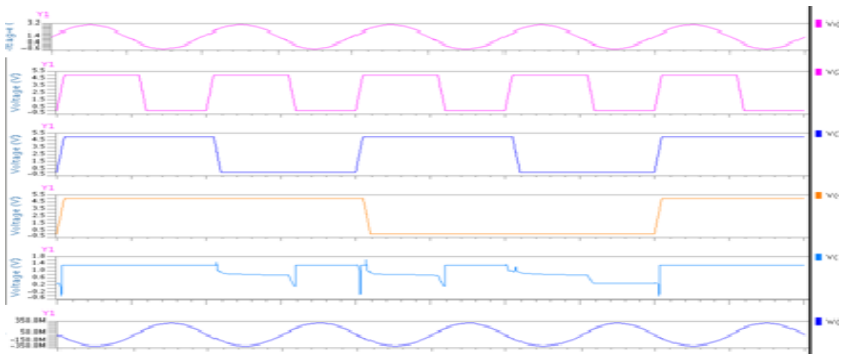

Fig. 28: Simulated Waveforms of 2PASCL Borrow

Fig. 28 shows the simulated waveforms of 2PASCL Borrow, where top and bottom signals are sinusoidal power clocks, the signals between them are three input signals and output signal respectively.

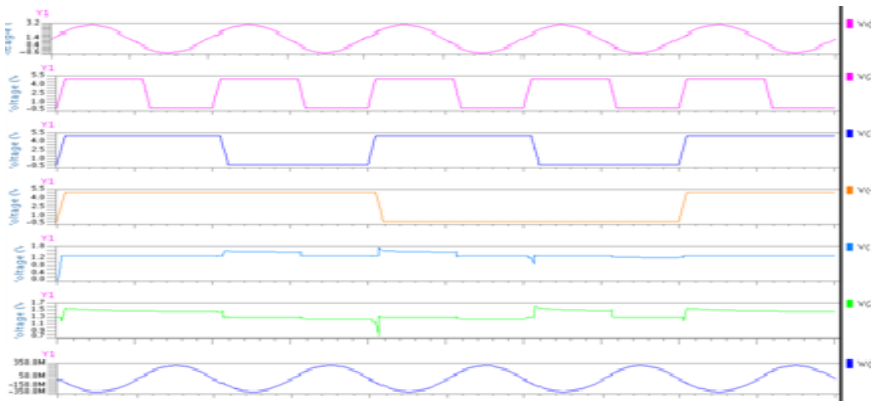

Fig. 29: Simulated waveforms of PFAL&2PASCL Difference

Fig. 29 shows the simulated waveforms of PFAL&2PASCL Difference, where top and bottom signals are sinusoidal power clocks, the signals between them are three input signals

and output signal respectively. Signal with constant amplitude refers to logic HIGH and signal with varying amplitude refers to logic LOW.

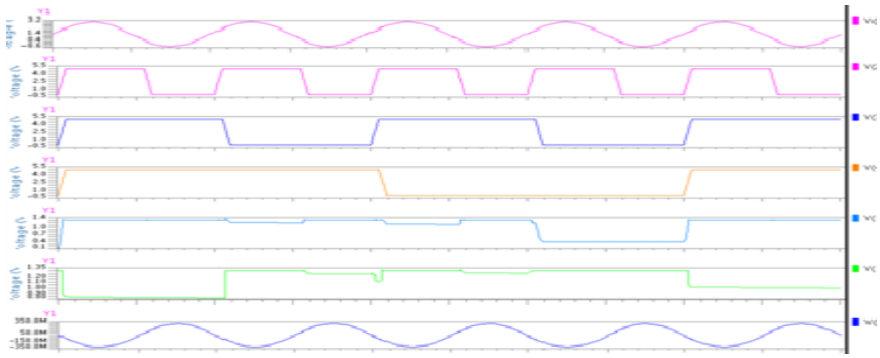

Fig. 30: Simulated Waveforms of PFAL&2PASCL Borrow

Fig. 30 shows the simulated waveforms of PFAL&2PASCL Borrow, where top and bottom signals are sinusoidal power clocks, the signals between them are three input signals and output signal respectively. Signal with constant amplitude refers to logic HIGH and signal with varying amplitude refers to logic LOW.

Table: 2: Comparison of different parameters of Full Subtractor in adiabatic logic with CMOS

	Logic style	Power dissipation (Watts)	Memory Space allocated(bytes)	Average no. of Newton iterations	Number of transistors	Latency (%)
DIFFERENCE	CMOS	3.1377E-10	43274240	4.127500	28	0.0000
	ECRL	4.2591E-07	43274240	4.865462	28	0.0000
	PFAL	1.2857E-10	43274240	4.671111	30	0.0000
	2PASCL	1.0448E-11	43274240	4.384416	28	0.0000
	PFAL&2PASL	3.7782E-11	43266048	4.371084	32	0.0000
BORROW	CMOS	1.9911E-10	43282432	3.638146	18	0.0000
	ECRL	6.5905E-07	43282432	4.655311	18	0.0000
	PFAL	1.3461E-06	43286528	4.225806	20	0.0000
	2PASCL	9.1542E-12	43282432	4.307487	18	0.0000
	PFAL&2PASL	2.8266E-11	43286528	3.988473	22	0.0000

Table 2 shows that the power dissipation of different adiabatic logic styles is lesser than the conventional CMOS design. The power supply that is given to the adiabatic circuits is also lesser than the conventional CMOS design

CONCLUSION

This paper proposes energy efficient adiabatic logic for digital circuits. The results were simulated using PSPICE at 50KHz and 50MHz frequency and comparison has been done for different parameters of full subtractor in different adiabatic logic styles and CMOS design. The results show that the proposed adiabatic logic has less power dissipation compared to conventional CMOS design and it also uses less power supply. These advantages made this logic more convenient for energy efficient digital applications.

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