
A Novel Structure of Unified Power Flow Controller Based Matrix Converter

Appala Narayana Rao, CH, K.D. Syam Prasad, Dr. Ch. Sai Babu, Sirisha Grandhi

Abstract— The main concept of unified power flow controller (UPFC) is based on back to back connection of two inverters with a common capacitor dc link. This capacitor brings about several disadvantages such as affecting the reliability of UPFC. This paper proposes a new topology for UPFC based on matrix converter. This configuration is combination of nine 4-quadrant switches and not any storage element. Main advantages of proposed topology are reduction of number of switches, low cost and size of UPFC. This operation of UPFC is tested and simulated on a single machine infinite bus (SMIB) using space vector modulation (SVM) technique. The UPFC is supposed to be operated on automatic power flow control mode.

Keywords— Matrix Converter, UPFC, FACTS Devices, SVM

I. INTRODUCTION

In recent years, due to economics' and environment problems, build of new power plant and transmission line become more difficult. Hence, it is advisable to enhance the power transfer capability of the existing transmission lines up to thermal limit instead of constructing new one. Simultaneous with develop of semiconductor technology, the flexible ac transmission systems (FACTS) devices is proposed by Hingorani [1]. The main aim of FACTS devices is rapid compensation and enhancement of flexibility of power line parameter. Some of the main FACTS controllers are static var compensator (SVC), thyristor control series capacitor (GCSC), static synchronous compensator (STATCOM) and static synchronous series compensator (SSSC). But, due to configuration, these controllers are not able to control the active and reactive power, separately. At the 90's decade, Gyugyi [2] proposed a multi objective compensator by the name of UPFC that is able to control and compensate each three significant parameters of transmission line, which are amplitude and phase of bus voltage and reactance of line, to control active and reactive power flow, separately. The UPFC is combination of STATCOM and SSSC which are connected back to back via a common dc link [2]. There is a large dc capacitor in the dc link that connects two voltage source inverter (VSI) to each other. The main role of dc capacitor is the control of power exchange between series and shunt terminals of UPFC. The cost and physical size of UPFC depends on rating of this dc link capacitor bank, considerably. Also, this capacitor has shorter life when compared to an ac capacitor of same rating, which limits the life and reliability of VSI's, too [3]. To overcome

this problem, indirect matrix converter (IMC) topology is used instead of UPFC's common topology [4, 5]. This topology removes dc capacitor from UPFC configuration, but it's main problem is fictitious dc link voltage control. In this context only one work has been reported [6] where the matrix converter is placed in series with the transmission line which leads to the

entire power being flowed through matrix converter so requires high power devices. The ability to link two regions with different frequencies, said by authors, is the advantage of series placement of matrix converter with transmission line, but this is a rare case in power system. Moreover, the mentioned construction in [6] may carry high currents flows from converter during faulty condition. In this paper an effort has been taken to replace the new configuration of UPFC based on matrix converter instead of common configuration. The matrix converter is placed shunt with transmission line and plays variable voltage source role that injected series with transmission line.

II. POWER SYSTEM OF PROPOSED UPFC

Fig.1. show the common configuration of three-phase matrix converter as an ac/ac converter

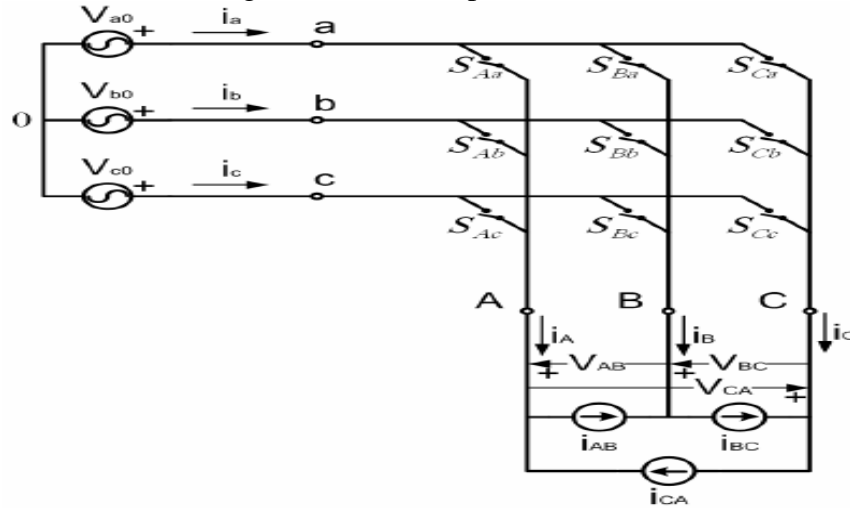


Fig 1. Three-phase matrix converter

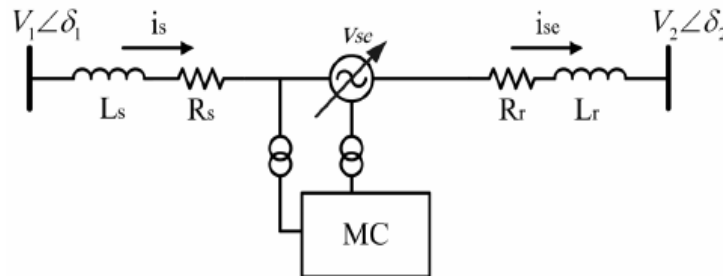


Fig. 2. Matrix converter placed as UPFC in the system

$$V_a = V_m \cos \theta_a = V_m \cos(\omega t)$$

$$V_b = V_m \cos \theta_b = V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \quad (1)$$

$$V_c = V_m \cos \theta_c = V_m \cos\left(\omega t + \frac{2\pi}{3}\right)$$

$$I_a = I_m \cos \theta_a = I_m \cos(\omega t - \psi_m)$$

$$I_b = I_m \cos \theta_b = I_m \cos\left(\omega t - \frac{2\pi}{3} - \psi_m\right) \quad (2)$$

$$I_c = I_m \cos \theta_c = I_m \cos\left(\omega t + \frac{2\pi}{3} - \psi_m\right)$$

Fig.1. show the common configuration of three-phase matrix converter as an ac/ac converter. The usual UPFC configuration [2] is replaced by a matrix converter that is placed in shunt combination with transmission line as shown in Fig. 2. The SMIB power system [7] is used for verifying the performance of proposed configuration of UPFC as shown in Fig. 3. The feeding network has been represented by it's Theremin's equivalent circuit on bus B1. The UPFC has been placed between B1 and B2 buses along transmission line (Fig. 3). The STATCOM side of the UPFC is connected in shunt with the transmission line using a step-down transformer. The SSSC side of the UPFC is connected in series with the transmission line. The basic operation of this side is to inject a voltage (v_{se}) of required magnitude, phase and frequency in series with transmission to control the active and reactive powers flow. This injected voltage is almost quadrant with the transmission line current. As a result, it plays the role of an inductance or capacitance in series [4]. A small phase difference existed from 90° between injected voltage and line current to supply the required losses in the coupling transformer and matrix converter. It is assumed that the input voltages of the matrix converter after the step-down shunt transformer are three-phase balanced sinusoidal voltages as follows;

$$\begin{aligned} V_u &= V_o \cos \theta_{ou} = V_o \cos(\omega t + \varphi_o + \psi_{out}) \\ V_v &= V_o \cos \theta_{ov} = V_o \cos\left(\theta_{ou} - \frac{2\pi}{3}\right) \\ V_w &= V_o \cos \theta_{ow} = V_o \cos\left(\theta_{ou} + \frac{2\pi}{3}\right) \end{aligned} \quad (3)$$

III. MODULATION TECHNIQUE

$$S_{jk}(t) = \begin{cases} 1, & S_{jk} \text{ closed} \\ 0, & S_{jk} \text{ open} \end{cases} \quad j \in \{A, B, C\}, k \in \{a, b, c\} \quad (4)$$

$$0 \leq s_{jk}(t) \leq 1, \quad \sum_{k=a}^c s_{jk}(t) = 1 \quad (j = A, B, C) \quad (5)$$

$$V_{oL} = \frac{2}{3} \cdot (v_{AB} + v_{BC} \cdot e^{+j120^\circ} + v_{CA} \cdot e^{-j120^\circ}) \quad (6)$$

In this technique, the matrix converter is separated into two parts, a VSI and a voltage source rectifier (VSR), which linked to each other via fictitious dc link.

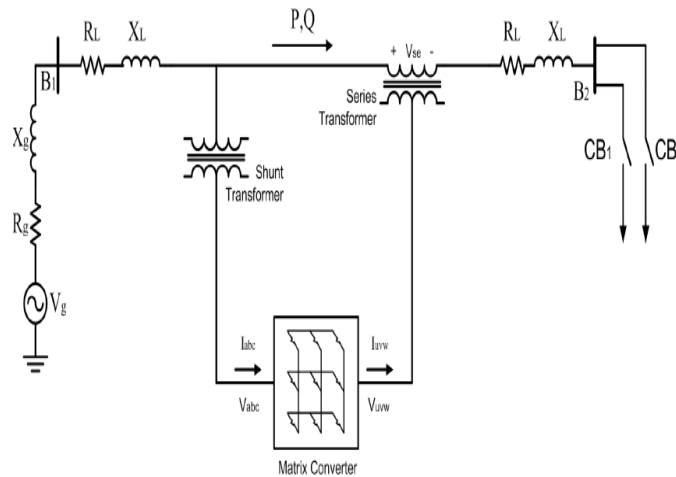


Fig. 3. Power system with the proposed scheme of UPFC

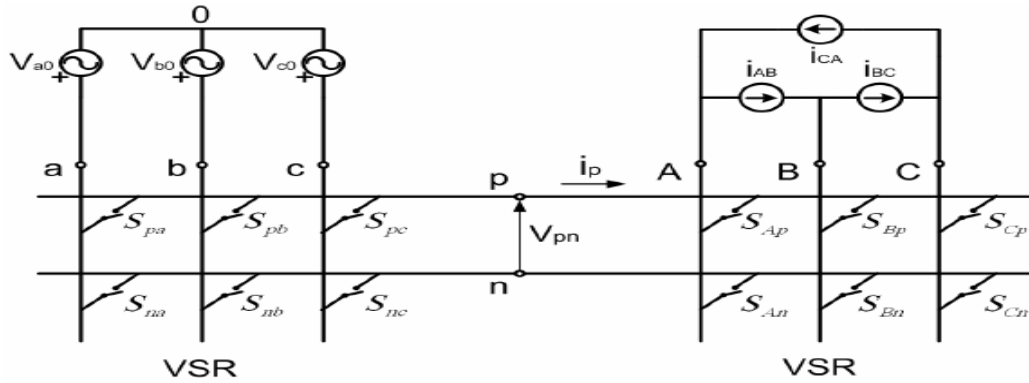


Fig. 4. Emulation of VSR-VSI conversion

The configuration of this approach is shown in Fig. 4. Here, the SVM technique is separately applied to the VSR and VSI part. This technique gives the duty cycles for the whole switches of each part. Then, the combination of these duty cycles gives the on/off switches states of matrix converter. Applying the ITF-SVM to matrix converter needs to be two separate SVM hexagon for each other, output voltage hexagon for VSI and input current hexagon for VSR, and then combined the resultant switching pattern to achieve the desired payoff (Fig. 5). The VSI switching patterns are as follows

$$d_\alpha = T_\alpha / T_s = m_v \cdot \sin(60^\circ - \theta_{sv}) \tag{7}$$

$$d_\beta = T_\beta / T_s = m_v \cdot \sin(\theta_{sv})$$

$$d_\mu = T_\mu / T_s = m_c \cdot \sin(60^\circ - \theta_{sc}) \tag{8}$$

$$d_v = T_v / T_s = m_c \cdot \sin(\theta_{sc})$$

where m_c is VSR input current modulation index and θ_{sc} is the desired input current angle. Since both the VSR and the VSI hexagons have six sectors, there are 36 combinations. If in a particular instant, the output voltage and input current be in the first sector of it's hexagon (Fig. 5), the output voltage could be synthesized by the pulse width modulation of the adjacent state space vectors $V1(p,n,n)$ and $V6(p,n,p)$. Also like this the input current state space vectors is $I1(a,c)$ and $I6(a,b)$, and the zero vectors is combination of $V0(n,n,n)$ or $V0(p,p,p)$ with $I0(a,a)$ or $I0(b,b)$ or $I0(c,c)$. The desired output voltage and input current is achieved with replaced the $I_i(p,n)$ into the $V_j(A,B,C)$.

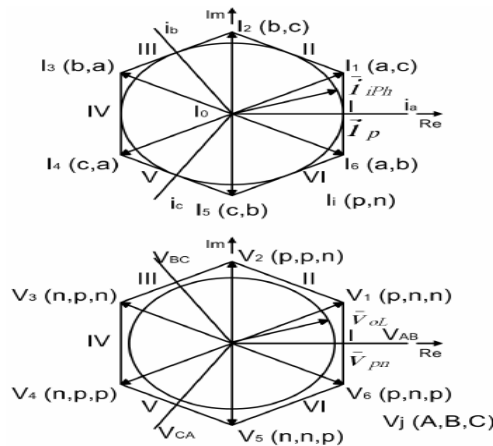


Fig. 5. Space vector modulation diagram

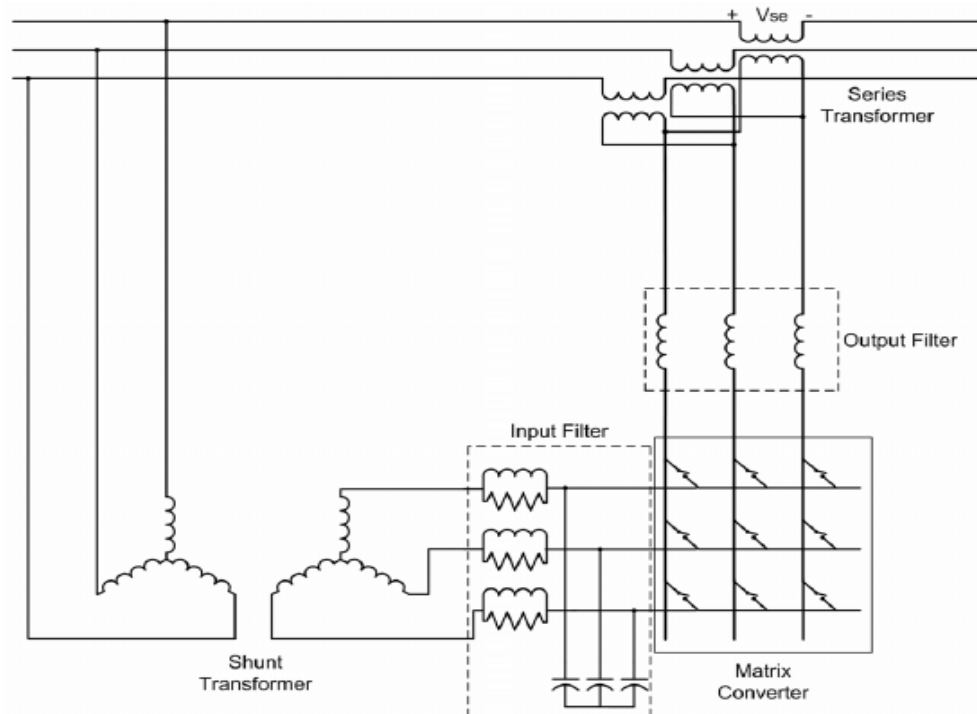


Fig. 6. Matrix converter in transmission line

$$\begin{aligned}
 T_{\alpha\mu} &= d_{\alpha} \cdot d_{\mu} \cdot T_s = m \cdot \sin(60^{\circ} - \theta_{sv}) \cdot \sin(60^{\circ} - \theta_{sc}) \cdot T_s \\
 T_{\beta\mu} &= d_{\beta} \cdot d_{\mu} \cdot T_s = m \cdot \sin(\theta_{sv}) \cdot \sin(60^{\circ} - \theta_{sc}) \cdot T_s \\
 T_{\alpha\nu} &= d_{\alpha} \cdot d_{\nu} \cdot T_s = m \cdot \sin(60^{\circ} - \theta_{sv}) \cdot \sin(\theta_{sc}) \cdot T_s \\
 T_{\beta\nu} &= d_{\beta} \cdot d_{\nu} \cdot T_s = m \cdot \sin(\theta_{sv}) \cdot \sin(\theta_{sc}) \cdot T_s
 \end{aligned} \tag{9}$$

To eliminate the high frequency component from input current and output voltage, passive filters are applied at two side of matrix converter (Fig. 6). The input side is connected by a filter and a Y – Y transformer to transmission line and the output through a filter and a Δ – Δ transformer [9].

IV. CONTROL SCHEME

The control of input bus voltage hasn't been attempted in this work. However, the input displacement factor of the matrix converter has been maintained close to unity. The controller is designed in a way that the UPFC operates in the automatic power flow control mode. Hence the reference inputs to the controller are Pref and Qref, which are to be maintained in the transmission line despite of system changes (Fig. 7.). A phase locked loop (PLL) is used to determine the instantaneous angle θ of the three-phase line voltage Vabc sensed at bus B2 of Fig. 3. The currents components Id and Iq of the three-phase line currents are used to determine the angle θ_{ir} relative to the voltage Vabc. From the actual line currents and voltages the active and reactive power flow over transmission line are determined. The Qerr obtained is stabilized through PI controller which generates the required small displacement angle β to control the angle of the injected voltage with respect to the transmission line current.

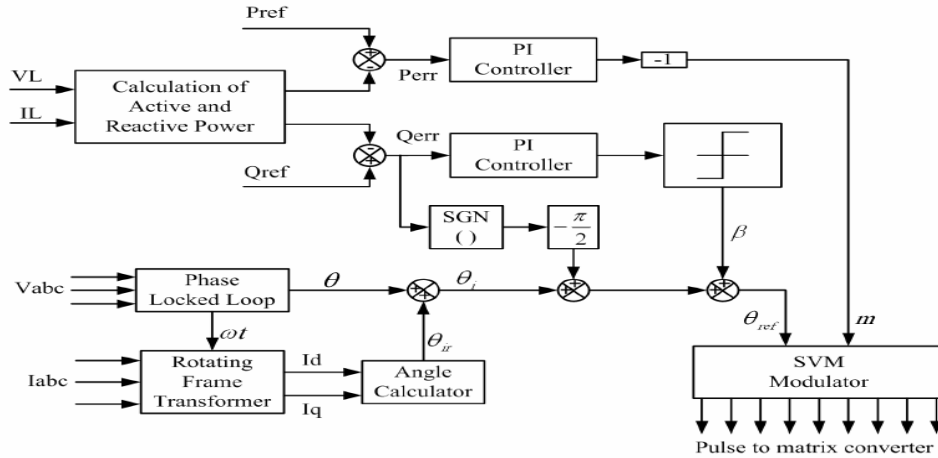


Fig. 7. Control block diagram of proposed

UPFC

Depending on the actual reactive power with respect to the desired value either $\pi/2$ is added (inductive) or subtracted (capacitive) with β . Thus, the desired phase angle is derived as $\theta_{ref} = \theta + \theta_{ir} + \beta \pm (\pi/2)$. The desired modulation index m and the phase angle θ_{ref} are applied to the SVM modulator.

V. SIMULATION RESULT

The parameters of the studied system (Fig. 3) are given in Table I. The UPFC is operated by using the automatic power flow control mode. In this mode, the UPFC can directly control the active and reactive power separately by controlling the amplitude and phase angle of the series injected voltage. The input voltage and current of UPFC are shown in Fig. 8. As shown in this figure, the voltage and current are almost in phase and this means that input power factor is near to unity.

The input voltage waveform contains high frequency harmonics which it is generated due to the switching and unfiltered output voltage injection to the transmission line. The output voltages and currents of UPFC are shown in Fig. 9.

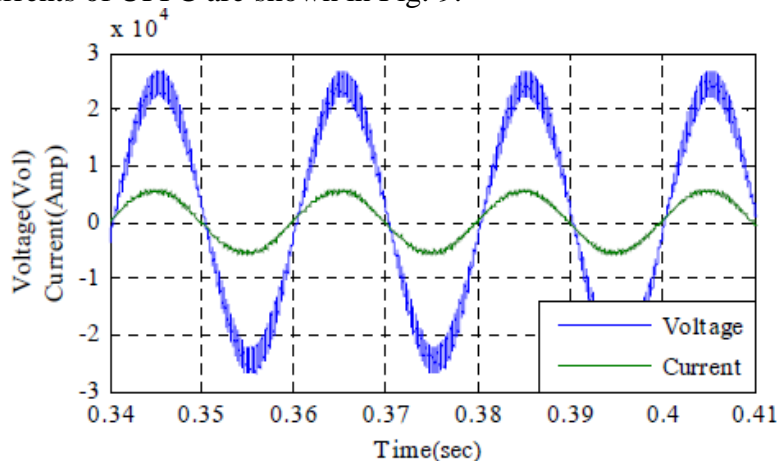


Fig. 8. Input voltage and current of UPFC

TABLE I
 Power System Parameters

Three-phase ac source	
Rated voltage	230 kV \times 1.03
Frequency	50 Hz
Short Circuit Level	10,000 MVA
Base voltage	230 kV
X_g/R_g	8
Transmission line	
Resistance per unit length	0.01755 Ω /km
Inductance per unit length	0.8737 mH/km
Capacitance per unit length	13.33 nF/km
Length	180 km
Shunt transformer	
Nominal power	150 MVA
Frequency	50 Hz
Nominal voltage	230 kV/27 kV
Magnetization reactance and resistance	500 p.u.
Series Transformer	
Rated voltage	42 kV/21 kV
Rated power	100 MVA
Magnetization reactance and resistance	500 p.u.
IGBT switches	
Internal resistance	0.001 Ω
Snubber resistance	0.1 M Ω
Snubber capacitance	Infinite

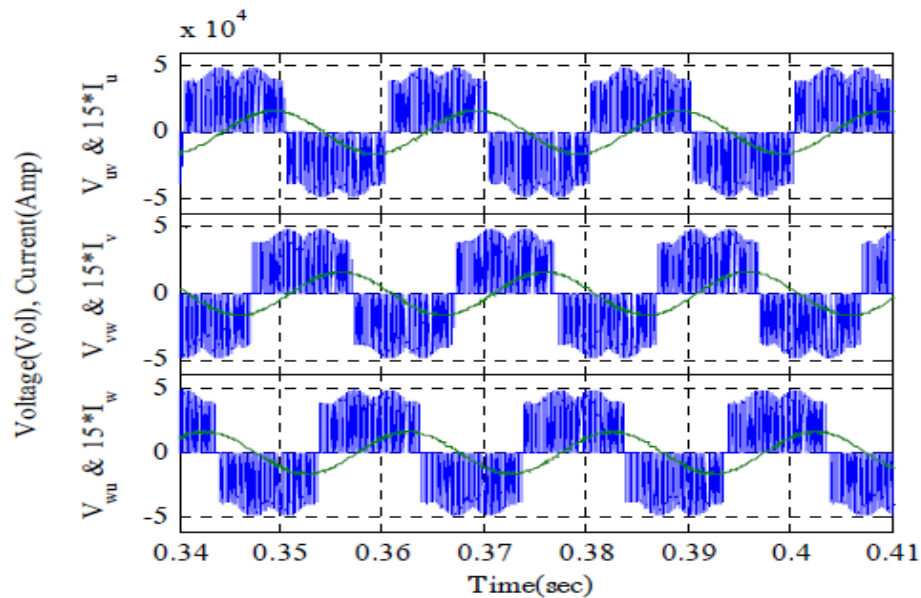


Fig. 9. Output voltage and current of UPFC

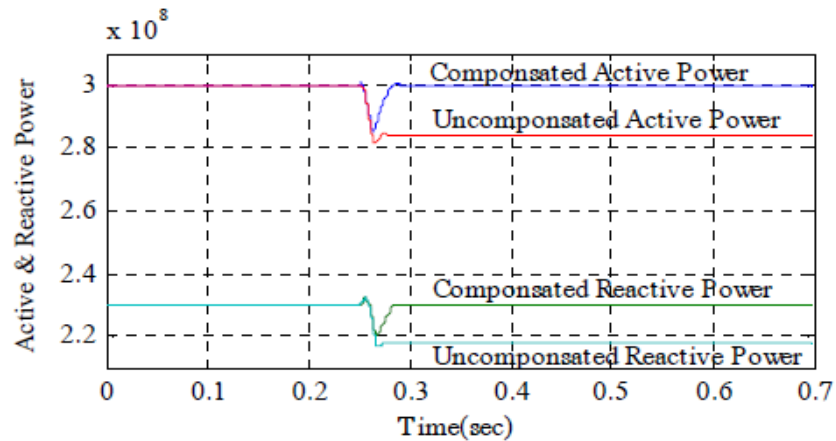


Fig. 10. Uncompensated and compensated power flow over the transmission line

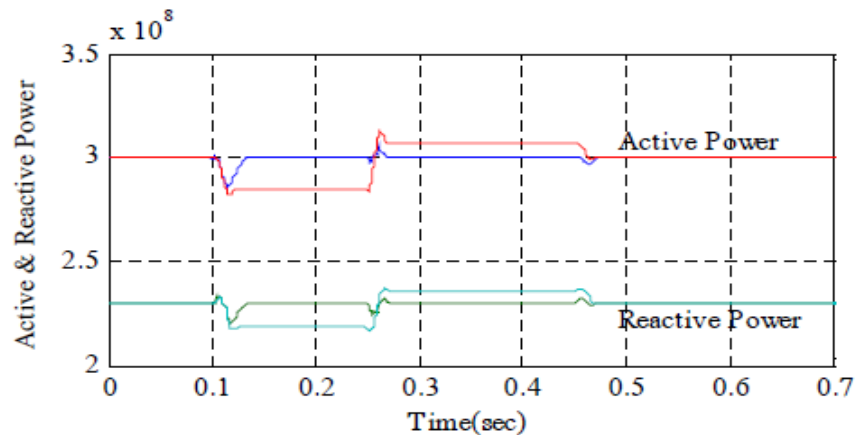


Fig. 11. Multi change in load value

This side of UPFC is connected directly, without any voltage filter, to series transformer. This voltage, which is injected in series with the transmission line, lags the line current almost by 90° , which shows that the series side of UPFC operates in inductive mode. A small deviation from 90° takes the active power flow from the transmission line in order to compensate the active power losses of the coupling transformer and the switches. Load variations due to faults are created to study the performance of the proposed scheme. The initial load in the system, equal in value with base power, is 300MW, 230MVAR and is disconnected at time 0.25s and other load with rating of 270MW and 205MVAR is applied to the system. P and Q of the transmission line track almost to the references irrespective of load variation as shown in Fig. 10. As shown in Fig. 10, the fallen area is due to the dynamic of transmission line and time response of PI controller. Moreover to test the performance of proposed scheme of UPFC, multi change of load is applied to the system and the result is shown in Fig. 11. that described the track of reference value of active and reactive power. A three-phase fault of 50ms duration is introduced in the transmission line at $t=0.25$ s and cleared at $t=0.3$ s. Due to fault voltage across UPFC's shunt side bus suddenly goes to zero as shown in Fig. 12a. This result in a corresponding output voltage and current in the series side of UPFC as depicted in Fig. 12b. However, P and Q of transmission line settles to the reference values within a small interval of time after the fault is cleared as described in Fig. 12c. These results clearly depict the transient

stability of the proposed model of UPQC

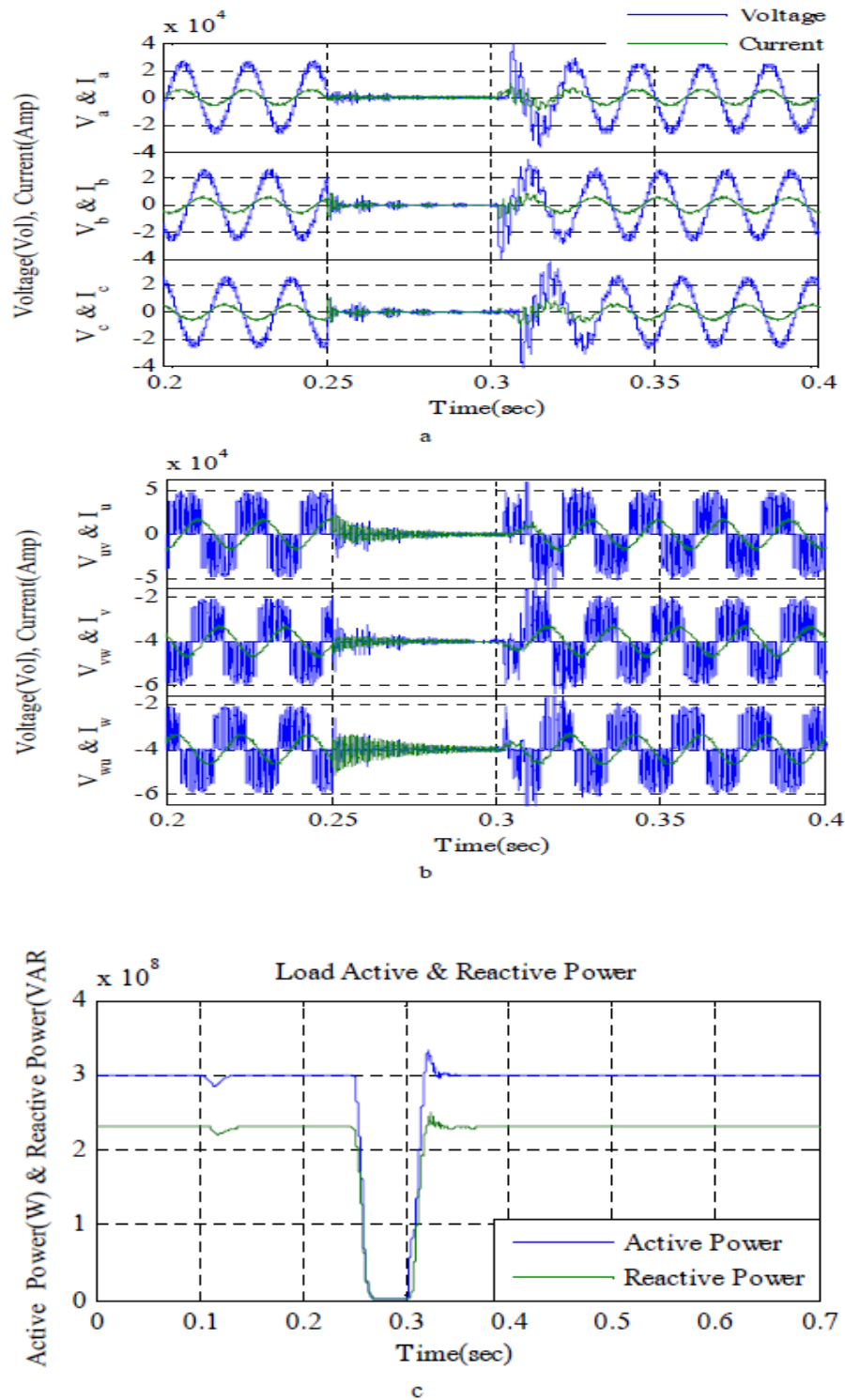


Fig. 12. Transient responses for a three-phase fault at infinite bus (a) line voltage and current in the shunt side, (b) output voltage and current in the series side and (c) active and reactive power flow over the transmission line.

VI. CONCLUSIONS

The contribution of this paper is to propose a new structure for UPFC based on matrix converter. This topology doesn't require dc-link energy storage elements. The cost and space occupied by the dc link capacitor in common UPFC structure are quite large. So the main advantage of proposed scheme is elimination of dc link capacitor. The dynamic performance of the proposed system is analyzed whereas assuming that the UPFC is connected to a 230kV transmission line of SMIB power system. In this scheme, the shunt side regulates the line voltage and the series side controls the magnitude and angle of the injected voltage in a way that the active and reactive power flow over the transmission line follows the set reference values in spite of variations in the load and the operating conditions.

REFERENCES

- [1] N. G. Hingoni, "High Power Electronics and Flexible AC Transmission System", IEEE Power Eng. Rev., vol. 8, no.7, July 1988.
- [2] L. Gyugyi, "Unified power flow control concept for flexible ac transmission systems", in *Proc. Inst. Elect. Eng.*, vol. 139: 323--331, 1992
- [3] Y. Minari, K. Shinohara and R. Veda, "PWM-rectifier/voltage-source inverter without DC link components for induction motor drives", IEE Proc. B on Elect. Power Appl., vol. 140, Issue 6, pp. 363-368, Nov.1993.
- [4] B. Geethalakshmi. P. Dananjayan, "Investigation of performance of UPFC without DC link capacitor", *Elect. Power Syst. Res.*, Vol. 78(4): 736-746, April 2008.
- [5] João Ferreira. Sónia Pinto, "P-Q Decoupled Control Scheme for Unified Power Flow Controllers Using Sparse Matrix Converters", 5th Int. Conf. on Euro. Elect. Mar., pp. 1-6, 28-30 May 2008.
- [6] B. T Ooi and M Kazerani, "Unified Power Flow Controller Based on Matrix Converter", 27th Annual IEEE Power Elect. Spe. Conf., Vol. 1, pp. 502-507, 23-27 June 1996.
- [7] M. S. El-Moursi and A. M. Sharaf, "Novel reactive power controllers for STATCOM and SSSC", *Elect. Power. Syst. Res.*, vol. 76, pp. 228-241, 2006.
- [8] L Huber and D Borojevic, "Space Vector modulated Three phase to Three phase Matrix Converter with Input Power factor Correction", *IEEE Trans. Ind. Appl.*, vol. 31, no. 6, pp. 1234--1246, 1995.
- [9] P. Mutschler and M. Marcks, "A Direct Control Method for Matrix Converters" *IEEE Trans. On Ind. Elect.*, vol. 49, no. 2, pp. 362-369, April 2002..

VII.AUTHORS



APPALA NARAYANA RAO.CH received his Master Degree in Power Systems in Electrical and Electronics Engineering, department of viswanada Institute of management and science Technology, mindivanipallem, anandapuram (md), Visakhapatnam (dt), India in 2013, Bachelor degree in Electrical and Electronics Engineering from T.P.I.S.T, Bobbili, Andhra Pradesh, India, in 2007.



K.D. SYAM PRASAD is working as Associate Professor and HOD in EEE department for VITAM College of Engineering, Visakhapatnam. He is pursuing PhD from JNTU Kakinada. His interested topics include Power Quality Management, wavelet transforms, FACTS controller and distributed systems.



Dr. Ch. Sai Babu received the B.E from Andhra University (Electrical & Electronics Engineering), M.Tech in Electrical Machines and Industrial Drives from REC, Warangal and Ph.D in Reliability Studies of HVDC Converters from JNTU, Hyderabad. Currently he is working as a Professor in Dept. of EEE in University College of Engineering, JNT University, Kakinada. He has published several National and International Journals and Conferences. His area of interest is Power Electronics and Drives, Power System Reliability, HVDC Converter Reliability, Optimization of Electrical Systems and Real Time Energy Management.



Sirisha Grandhi received her B.Tech degree in Electrical & Electronics Engineering from Narayana Engg College Nellore, Andhra Pradesh, India in 2007 and M.Tech degree from Jntuk Kakinada in High Voltage Engineering, in 2010. Currently she is working as Assistant Professor in the Department of Electrical and Electronics Engg., Jyothishmati College of Engineering, Thurkapally, R.R.District, Andhra Pradesh India.