DESIGN OF HIGH PERFORMANCE DIGITAL CMOS PARALLEL COUNTER

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ABSTRACT

In this project, the counter operating frequency is improved by using a novel parallel counter architecture in conjunction with a state look-ahead path and pipelining. This is proceeded to eliminate the carry chain delay and reduce AND gate fan-in and fan-out. Here only three simple CMOS logic modules are used. These three modules are placed in a highly repetitious structure in both the counting path and state look-ahead path. An initial module generates anticipated counting states for higher significant bit modules through the state look-ahead path. In order to achieve high operating frequency a high speed parallel counter is presented. The design can be implemented using CADENCE-90nm CMOS technology.

Keywords: —Architecture design, high-performance counter design, parallel counter design, pipeline counter design.

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1. INTRODUCTION

Counters are widely considered as essential building blocks for a variety of circuit operations. The parallel counter architecture design is used to achieve high operating frequency through a novel pipeline partitioning methodology. The 8-bit parallel counter is partitioned into four 2-bit synchronous counter. Here using only three simple repeated CMOS logic module types .These three modules are placed in a highly repetitious structure in both the counting path and state look-ahead path. The state look-ahead logic avoids the use of an overhead delay detector circuit. The counting path's counting logic controls counting operation .The state look-ahead path's state look-ahead logic anticipates future states and thus prepares the counting path for these future states .In the parallel counter architecture design, all counting modules are concurrently transition to their next states at the rising clock edge.

The objective of this project is to improve the counter operating frequency by eliminating the carry chain delay and reduce the AND gate fan-in and fan-out.

2. PARRALLEL COUNTER ARCHITECTURE

The proposed parallel counter architecture for a sample 8-bit counter. The main structure consists of the state look-ahead path (all logic encompassed by the dashed box) and the counting path (all logic not encompassed by the dashed box).We construct our counter as a single mode counter, which sequences through a fixed set of preassigned count states, of which each next count state represents the next counter value in sequence.

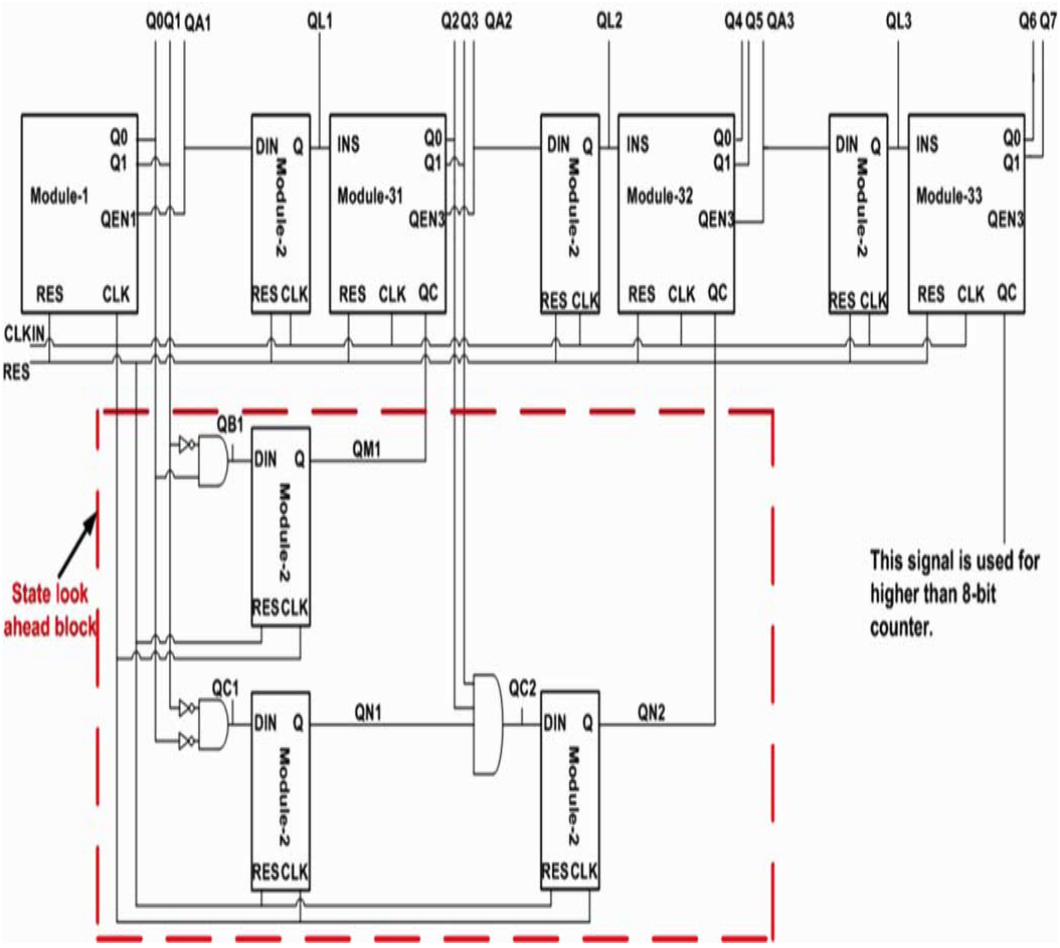

Fig 1: Block Diagram of 8-Bit Parallel Counter

The counter is partitioned into uniform 2-bit synchronous up counting modules. Next state transitions in counting modules of higher significance are enabled on the clock cycle preceding the state transition using stimulus from the state look-ahead path. Therefore, all counting modules concurrently transition to their next states at the rising clock edge (CLKIN).

A.Architectural Functionality

The counting path's counting logic controls counting operations and the state look-ahead path's state look-ahead logic anticipates future states and thus prepares the counting path for these future states. The three module types (module-1,module-2,module-3S).Module-1 and module-3 are exclusive to the counting path and each module represents two counter bits.Module-2 is the conventional positive edge triggered DFF and is present in both paths.

In the counting path, each module-3 is preceded by an associated module-2. Module-3 's serve two main purposes. Their first purpose is to generate all counter bits associated with their ordered position and the second purpose is to enable (in conjunction with stimulus from the state look-ahead path) future states in subsequent module-3 's in conjunction with stimulus from the state look-ahead path. The counter architecture consists of two parts.

Counting path: The counting path consists of module-1, module-2 and module-3.The counting path is the way to count sum of all paths from the lower order count to the higher order count. The counting path module-1 is responsible for lower- order bit counting and generates future states for all module-3's by pipelining, the enable for these futures states through the state look-ahead path. The placement of module-2s in the counting path is critical to the novelty of counter structure. Module-2s in the counting path act as a pipeline between the module-1 and module-3 1 and between subsequent module- 3S.

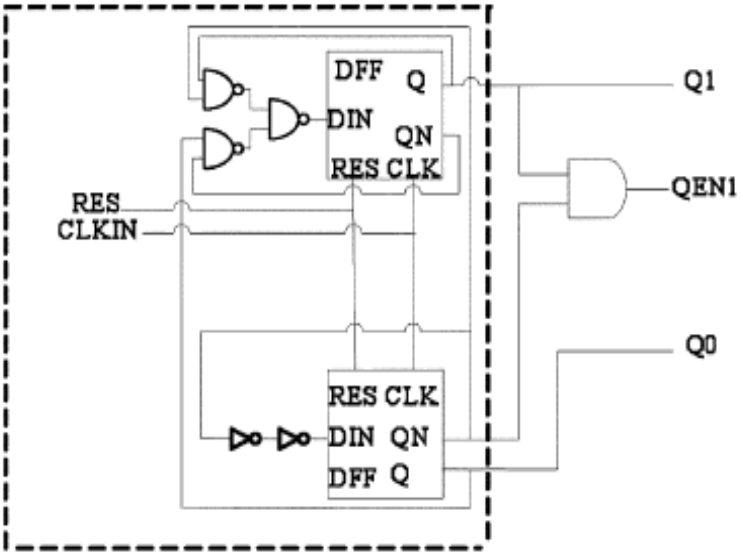

Fig 2: Hardware Schematic Diagram of Module-1

The module-2s in the counting path provide a 1-cycle look-ahead mechanism for triggering the module-3S, enabling the module-2s to maintain a constant delay for all stages and all module-3S to count in parallel at the rising clock edge instead of waiting for the overflow rippling in a standard ripple counter. The module-1 outputs Q1Q0 and QEN1=Q1 AND Q0. QEN1 is connects to the module-2's DIN input.

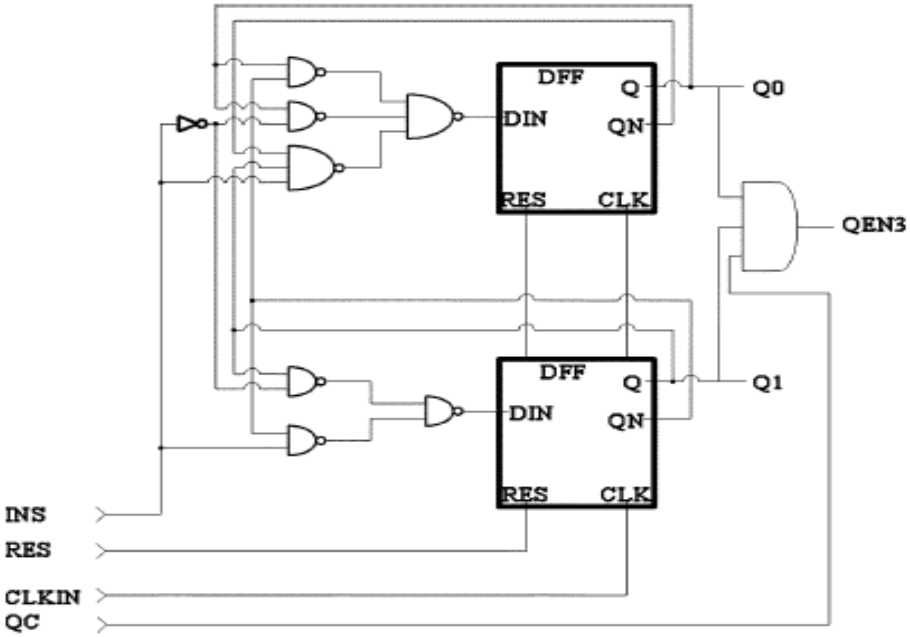

Fig 3: Hardware Schematic Diagram of Module-3

State Look-Ahead Path: The state look-ahead path operates similarly to a carry look-ahead adder in that it decodes the low-order count states and carries this decoding over several clock cycles in order to trigger high-order count states. The state look-ahead logic is principally equivalent to the one-cycle look-ahead mechanism in the counting path. The placement of module-2 in the state look-ahead logic increases counter operating frequency by eliminating the lengthy AND-gate rippling and large AND gate fan-in and fan-out typically present in large width parallel counters. The enabling next state's high- order bits depends on early overflow pipelining across clock cycles through the module-2s in the state look-ahead path. This state look-ahead logic organization and operation avoids the use of an overhead delay detector circuit that decodes the low order modules to generate the enable signals for higher order modules, and enables all modules to be triggered concurrently on the clock edge, thus avoiding rippling and long frequency delay.

Table 1: RELEVANT INTERMEDIATE SIGNAL (SEE FIG. 1) VALUES FOR COUNTER STATES 0–15

		Intermediate Signals									
clk	Q7Q6Q5 Q4Q3Q2 Q1Q0	QA1	QB1	QC1	QL1	QM1	QN1	QA2	QC2	QL2	QN2
0	00000000			$\bar{q}1q0$							
1	00000001		$\bar{q}1q0$				$\bar{q}1q0$				
2	00000010	$q1\bar{q}0$				$q1\bar{q}0$					
3	00000011				$q1q0$						
4	00000100			$\bar{q}1q0$							
5	00000101		$\bar{q}1q0$				$\bar{q}1q0$				
6	00000110	$q1\bar{q}0$				$q1\bar{q}0$					
7	00000111				$q1q0$						
8	00001000			$\bar{q}1q0$							
9	00001001		$\bar{q}1q0$				$\bar{q}1q0$				
10	00001010	$q1\bar{q}0$				$q1\bar{q}0$					
11	00001011				$q1q0$						
12	00001100			$\bar{q}1q0$							
13	00001101		$\bar{q}1q0$				$\bar{q}1q0$		$q3q2$ $\bar{q}1q0$		
14	00001110	$q1\bar{q}0$				$q1\bar{q}0$		$q3q2$ $q1\bar{q}0$			$q3q2$ $q1\bar{q}0$
15	00001111				$q1q0$					$q3q2$ $q1q0$	

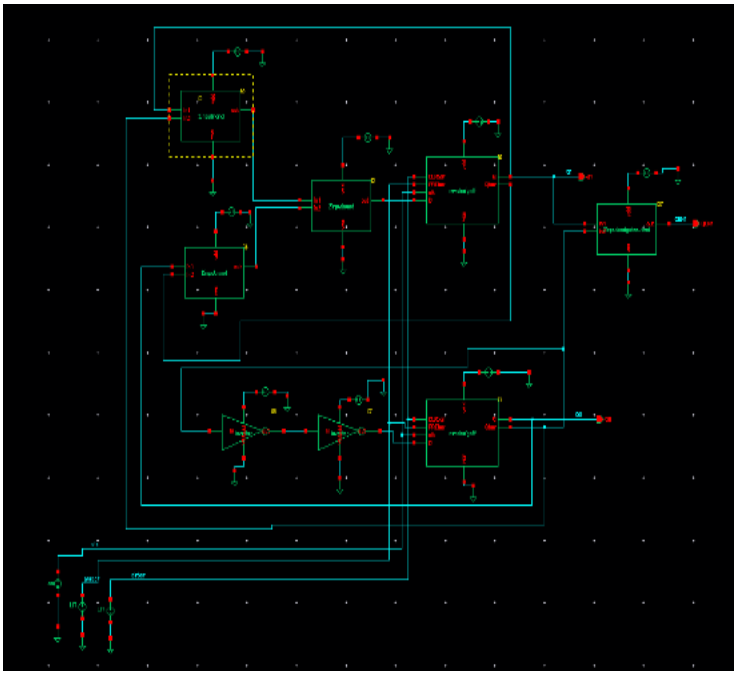

Fig 4: Schematic Diagram of Module-1

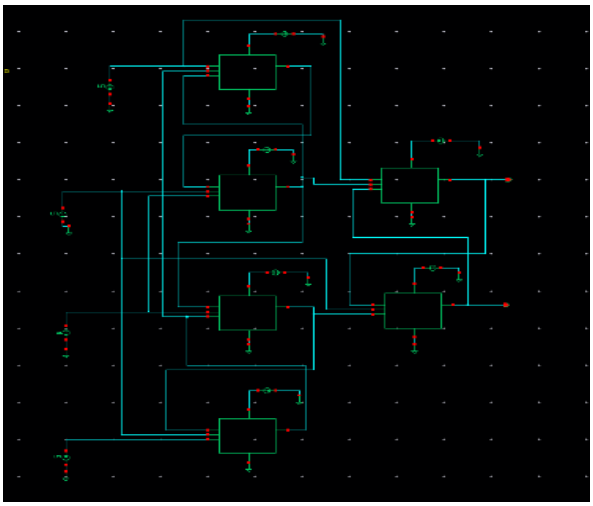

Fig 5:Schematic Diagram of Module-2

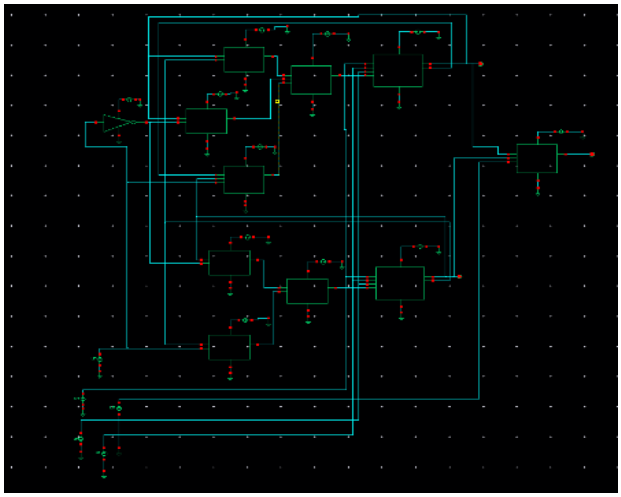

Fig 6: Schematic Diagram of Module-3

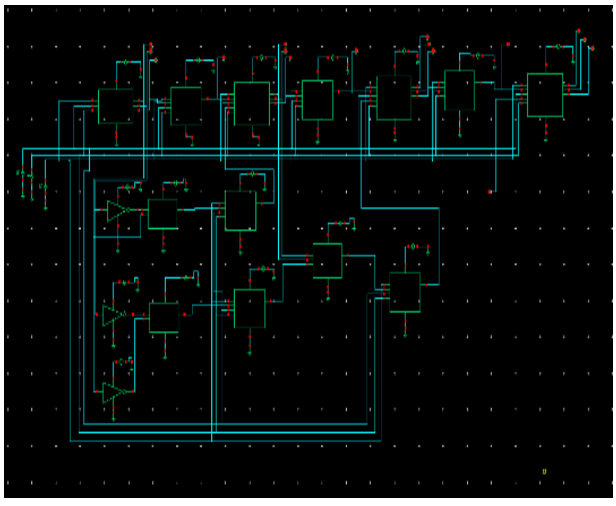

Fig 7: Schematic Diagram of Parallel Counter

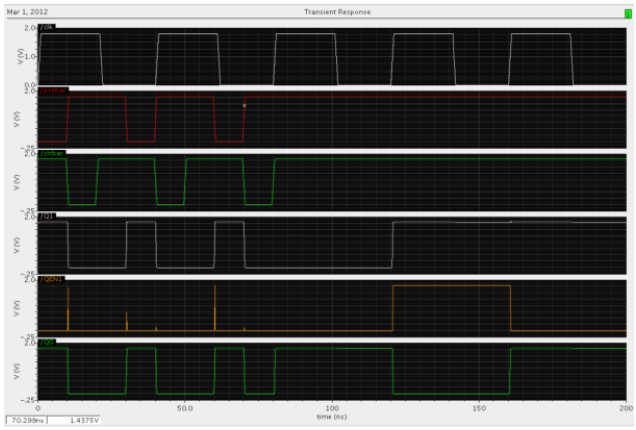

Fig 8: Output Waveform of Module-1

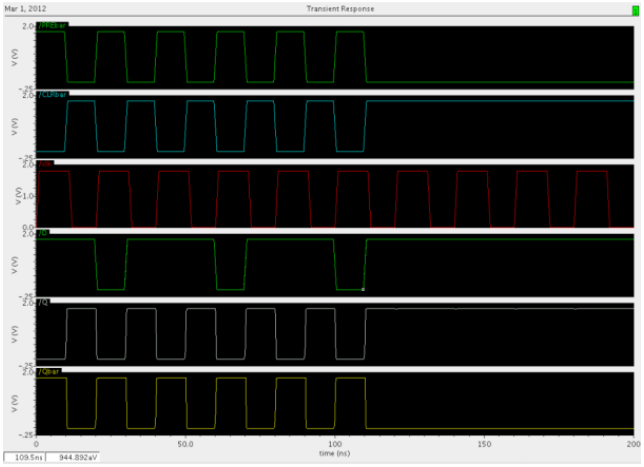

Fig:9 Output Waveform of Module-2

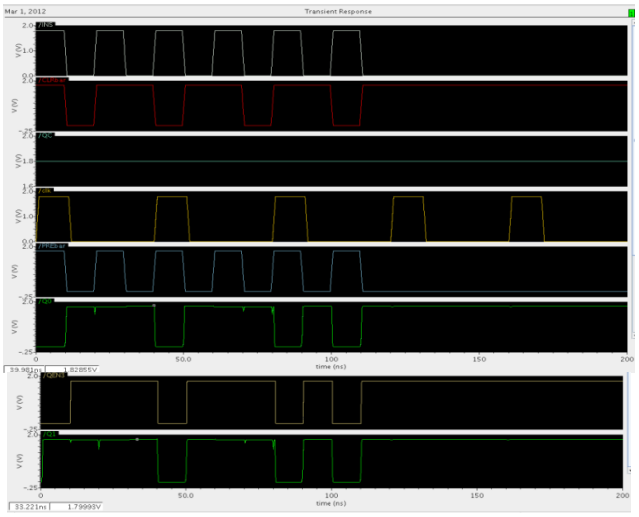

Fig 10: Output Waveform of Module-3

Fig 11: Output Waveform of Parallel Counter

CONCLUSION

The counter structure's main features are a pipelined paradigm and state look-ahead path logic whose inter operation activates all modules concurrently at the system's clock edge, thus providing all counter state values at the exact same time without rippling effects. This structure avoids using a long chain detector circuit typically required for large counter width.

In addition, this structure uses a regular VLSI topology, which is attractive for continued technology scaling due to two repeated module types forming a pattern paradigm

and no increase in fan-in or fan-out as the counter width increases resulting in a uniform frequency delay that is attractive for parallel designs. Consequently, the counter frequency is greatly improved by reducing the gate count on all timing paths to two gates using advanced circuit design techniques.

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