

## Spice Electro-thermal Behavioral Model for a Silicon Carbide Power MOSFET

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### ABSTRACT

This paper presents a new behavioral model for power MOSFET in silicon carbide (SiC); a model based on elements of the Spice library ABM (Analog Behavioral Models) which render it very flexible and easily integratable into the various Spice-based simulation softwares (BSIM, OrCAD, LTSpice, etc). The model parameters are extracted from the manufacturers' data (data sheets curves) by using the polynomial interpolation together with methods of simulated annealing (SA) and weighted least squares (WLS). This model takes into account the various important phenomena taking place within the transistor. Whereas the thermal behavior is epitomized by using the Foster canonical localized network extracted from the electro-thermal curve measurement (datasheet). This model is valid for all types of power MOSFET. Its relevance has been supported by very satisfactory results found in six references.

**Key words:** SiC power MOSFET, Electro-thermal Model, ABM, SPICE Modeling, Behavioral Model

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### INTRODUCTION

Nowadays, simulation has become a standard tool in the development and optimization of power electronic circuits. For these circuits, the temperature raise in power is one of phenomena that are very difficult to control. These new components (based on SiC) are characterized by excellent heat resistance [1], excellent electrical properties [2], and operate at high power levels and high switching frequencies [3]. Among them are the MOSFET transistors which are now very predominant in a large part of the industry. That's why modeling these components is of so much significance to us.

Unfortunately, the SiC MOS transistors are still in an ongoing development and so are the existing models as a result [4]. Therefore; one must take into account all the important phenomena occurring in these components. The precise prediction of the component behavior in high power is required for designing a robust and reliable power supply and for delimiting electromagnetic interferences (EMI) [5].

Most existing models provided by the manufacturers or traditional libraries simulators (such as OrCAD Spice) are based on physical equations of the semiconductor [6] [7] [8]. They are either simple but imprecise or otherwise multifarious and complex. Therefore; the behavioral modeling remains the easiest way to adequately describe the operativeness of the component [9] as will be shown below.

## THE POWER SiC MOSFET MODEL

### Presenting the model

The behavioral modeling provides a system response without knowing what it contains within it [10]. It is used to reduce the complexity of the model. Its implementation has become specific for each platform: MAST language for Saber; ABM library for SPICE; and functional blocks for Matlab.

The component model takes into account the most important phenomena of the MOS as shown in Figure 1 (Fig.1). It Includes voltage controlled voltage sources (VCVS) represented as "Ei", voltage controlled current sources (VCCS) represented as "Gi" [11], resistors, and capacitances. The values and parameters of its elements are determined according the interpolation curves provided by the manufacturer.

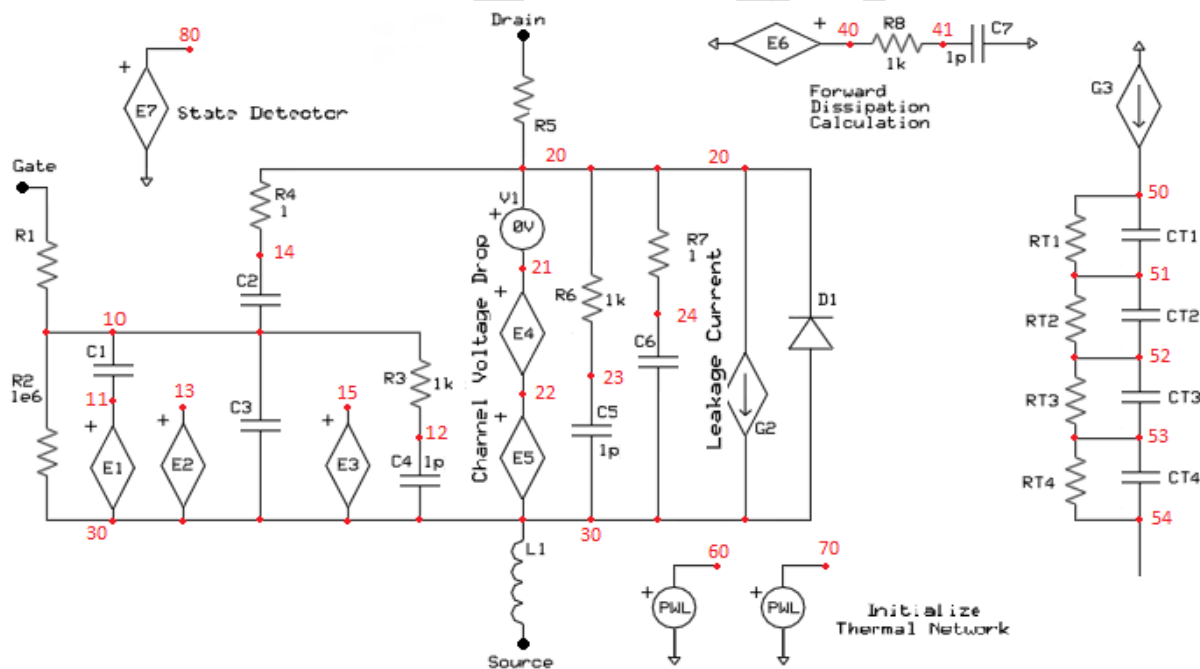


Fig1. the Subcircuit Diagram proposed SiC power MOS behavioral model

The modeled effects of the transistor according to the junction temperature are:

- Input admittance
- Dynamic capacitances
- Forward Conduction Voltage drop
- Forward blocking Leakage current  $I_{DSS}$

- Thermal impedance

### MOS input admittance

Viewed from the gate, MOS transistor behaves as a current source  $I_D$  controlled by a voltage  $V_{GS}$ . This dependence ( $I_D(V_{GS})$ ) is represented by the input admittance. The static characteristic of  $I_D(V_{GS})$  can be regarded as linear in a certain voltage threshold ( $V_{GSth}$ ) (Fig. 2). While below, the model is quadratic [11].

$$I_D = K \cdot (V_{GS} - V_{GS(th)})^2 \quad (1)$$

The linear part is modeled by E3 (Voltage Controlled Voltage Source VCVS) (Fig.1). The equation of the control voltage (2) is dependent on the junction temperature (polynomial of degree 2).

$$V_{E3} = (Ga_0 + Ga_1 \cdot V(T) + Ga_2 \cdot V(T)^2) + (Gb_0 + Gb_1 \cdot V(T) + Gb_2 \cdot V(T)^2) \times V_{C4} \quad (2)$$

$Ga_0$ ,  $Ga_1$ ,  $Ga_2$ ,  $Gb_0$ ,  $Gb_1$ , and  $Gb_2$  are polynomial coefficients interpolating polynomial curves (typical transfer characteristics  $I_D(V_{GS})$  depending on the temperature) of the manufacturer data (Fig.2).

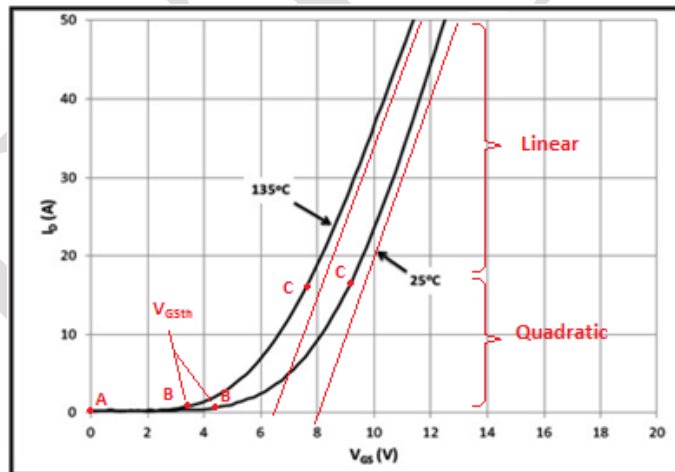


Fig 2 : Input Admittance Characteristics  $I_D(V_{GS})$

### MOS dynamic capacitances

The power MOSFET has three inter-electrode capacitances: the input capacitance ( $C_{iss}$ ), the reverse capacitance ( $C_{rss}$ ) and the output capacitance ( $C_{oss}$ ) (Fig.3) whose values are associated with pairs of terminals (i.e. Gate, Drain and Source) by the following equations [13].

- $C_{GS} = C_{iss} - C_{rss}$
- $C_{GD} = C_{rss}$  (3)

-  $C_{DS} = C_{oss} - C_{rss}$

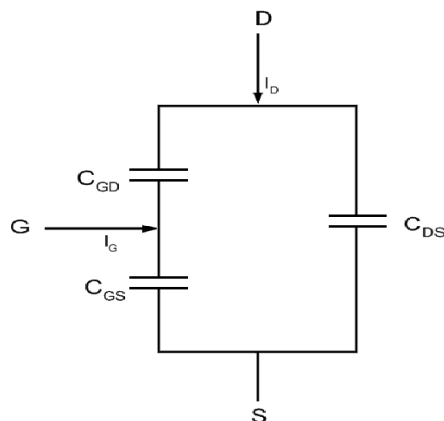


Fig 3 : Power MOS dynamic capacitances

The  $C_{rss}$  is the most preminent of these capacitances since it dominates the drain switching waveforms through the "Miller" effect. The capacitances  $C_{GS}$  and  $C_{GD}$  are loaded and unloaded through the gate control circuit, enabling the switch to occur and making the rise and fall timing (switching) of  $V_{DS}$  very dependent on the current value of the Gate. Indeed; several models have been adopted to model the nonlinearities of these capacitances [14] [8].

In an inductive load circuit,  $I_D$  remains essentially constant during switching which maintains  $V_{GS}$  constant [13], according to the input admittance (linear model  $I_D(V_{GS})$ ).

During switching, the  $V_{GS}$  amplitude can be divided into three distinct regions (Fig.4) each is specific to a definite switching phase [13] [15].

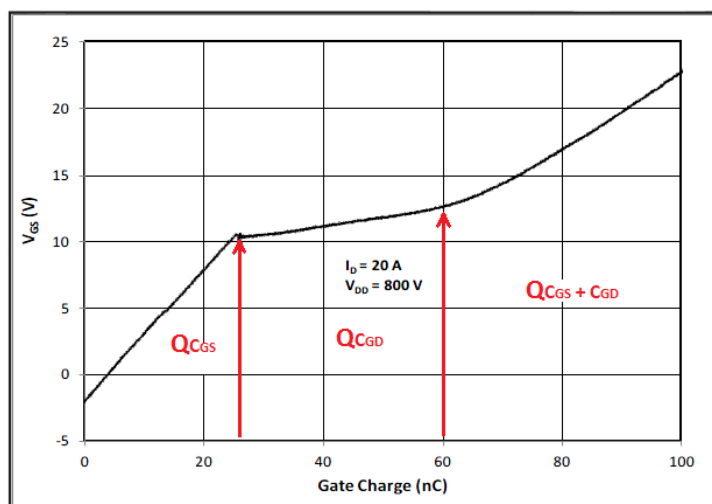


Fig 4 : MOS gate charge curve with region boundaries V<sub>GS</sub>(gate charge)

**Region 1** (0-25C) includes the delay in the conduction and rise of drain current from zero to its  $I_D$  value in the on-state.

**Region 2** (25 nC and 60 nC): During this phase  $V_{GS}$  increases slightly in an almost constant rate due to the  $C_{GD}$  and Miller effect, whereas  $V_{DS}$  goes down from its value proper to zero and  $V_{GS}$  remains almost constant. As a result all the current control circuit in the gate flows to  $C_{GD}$  (discharge).

**Region 3** (from 60 nC): This phase occurs when  $V_{DS}$  reaches the Ohmic region and the control current becomes again capable of loading  $C_{GS}$  and  $C_{GD}$  which become then in parallel with the voltage control of the Gate ( $V_{GS}$ ).

The dynamic capacitances of the MOS are represented in this model by four capacitors  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_6$  and two voltage controlled voltage sources (VCVS)  $E_1$  and  $E_2$  (Fig.1). Their values are determined according to the datasheet curves (capacity- $V_{DS}$  Fig.5) as follows.

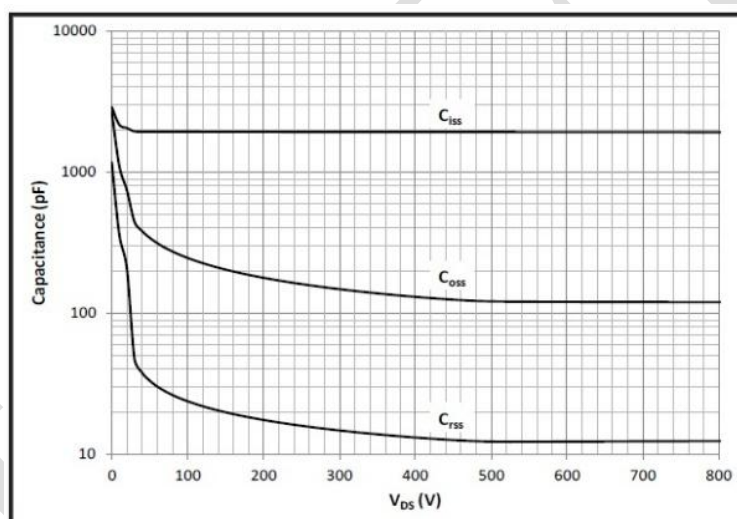


Fig 5 : MOS dynamic capacitance curves

- $C_2$  is the  $C_{GD}$  capacitance ( $C_{rss}$ ) in the highest voltage  $V_{DS}$  (here  $V_{DSmax} = 800V$ ).
- $C_3$  is the  $C_{GS}$  capacitance which has the value of  $C_{iss} - C_{rss}$  in the highest voltage  $V_{DS}$  (here  $V_{DSmax} = 800V$ ).
- $C_1$  is the  $C_{GD}$  ( $C_{rss}$ ) capacitance at the zero voltage  $V_{DS}$  ( $V_{DS} = 0V$ ).
- $C_6$  is the  $C_{DS}$  capacitance which has the value of  $C_{oss} - C_{rss}$  at the highest voltage (here  $V_{DSmax} = 800V$ ).
- $E_2$  is voltage controlled voltage source  $V_{DS} = V_{C5}$  that keeps its value to 1 when  $V_{DS}$  reaches its maximum value.
- $E_1$  is voltage controlled voltage source of the output of  $E_2$ .

The VCVS  $E_1$  follows  $V_{GS}$  when  $V_{DS}$  reaches its maximum value. At this stage, the capacitance  $C_1$  has a zero voltage at its terminals. ( $V_{C1} = 0V$ ),  $V_{DS}$  diminishes down  $V_{DSmax}$  and the voltage  $V_{E1}$  (output of  $E_1$ ) goes to 0 which ultimately results in a potential difference at the terminals of  $C_1$  receiving a current from  $C_2$  ( $C_2$  discharge).

### Forward Conduction Voltage drop

According to the input admittance relationship  $I_D(V_{GS})$  described above (1),  $V_{GS}$  becomes higher than  $V_{GSth}$  (when the device shifts into its active region) (Fig.6). When the current  $I_D$  boosts the device turns into its ohmic region which is the end of the switching. In this state, the MOS is on and is characterized by a minimal drop of  $V_{DS}$  voltage according to equation (4):

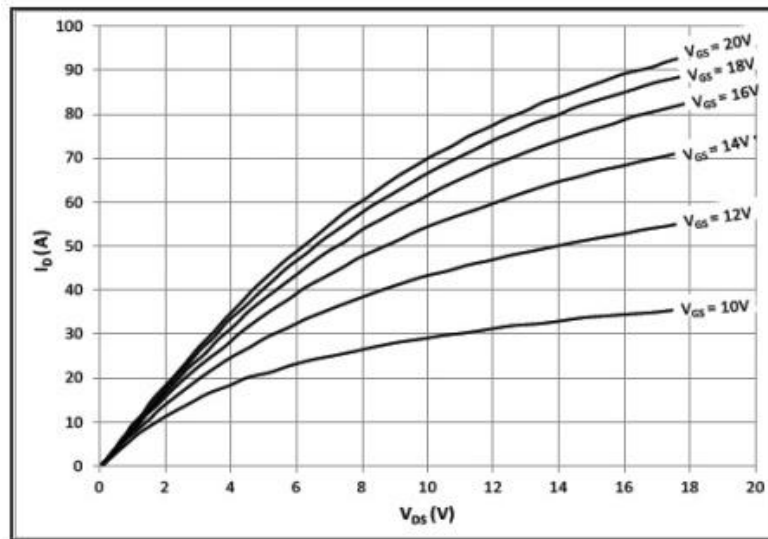


Fig 6 : Output characteristics as a function of gate voltage for 135 °C.

$$V_{DS} = R_{DSon} \times I_D \quad (4)$$

$R_{DSon}$  represents the sum of the multiple MOS resistances: R-channel, R-source, R-substrate and the epitaxial region resistance. The latter is the most important component for  $V_{DS}$  at 500 V and more [13]. The Ohmic region forms the linear part of the curves  $I_D(V_{DS})$  at  $V_{GS} = \text{const.}$  The slope in the curve indicating the  $R_{DSon}$  value is provided by the following equation (5).

$$R_{DSon} = \frac{\Delta V_{DS}}{\Delta I_D} \quad (5)$$

In this model, the drop voltage drain-source  $V_{DS}$  consists of two parts: the first is represented by the source E4 (Ohmic region) and the second by the source E5 (the active region).

The equation of the control voltage source E4 is provided by the following equation (6).

$$V_{E4} = (Ra_0 + Ra_1.V(T)) + (Rb_0 + Rb_1.V(T)) \times I(V_1) + (Rc_0 + Rc_1.V(T)) \times I(V_1)^2 \quad (6)$$

$Ra_0$ ,  $Ra_1$ ,  $Rb_0$ ,  $Rb_1$ ,  $Rc_0$  and  $Rc_1$  are the polynomial coefficients of the polynomial interpolation using the intersection line of the three curves of the gate drive  $V_{GS} = 16V$ ,  $V_{GS} = 18V$  and  $20V$  at 25 °C and 125 °C (Fig.10).

$I(V1)$  is the drain current flowing in  $V1$  (Fig.1). The output of  $E4$  is the ramp limited by the maximum value of the ohmic region (20V, 100A)

The  $E5$  VCVS is the amplified error produced by the drop voltage of drain-source limiting  $I_D$  to the value determined by the input admittance ( $E3$ ) as the following equation shows (7).

$$V_{E5} = Gain(I_D - I_{adm}) \quad (7)$$

$I_{adm}$  represents the maximum value of the drain current and is dependent on the  $V_{GS}$  and temperature which the component can withstand (this value determined by  $E3$ ). The output ramp is also  $E5$ .

### MOS Forward blocking Leakage current $I_{DSS}$

The datasheets of these power MOSFETs in SiC contain no figure illustrating the characteristics of the leakage current in the off- state. But- under some conditions- they give the absolute maximum value of leakage current  $I_{DSS}$  for all the analyzed transistors (C2M0025120D CREE [16], C2M0160120D CREE [17], C2M1000170D CREE [18], CMF10120D CREE [19], CMF20120D CREE [20], and SCT30N120 STMicro [21]) as shown in the following table (Table.1).

TABLE I. Forward blocking Leakage current  $I_{DSS}$  and power dissipit for the six analyzed transistors

	<i>C2M0025120D CREE</i>	<i>C2M016012 0D CREE</i>	<i>C2M1000170 D CREE</i>	<i>CMF10120 D CREE</i>	<i>CMF20120D CREE</i>	<i>SCT30N120 STMicro</i>
$V_{DS}$	1200 V	1200 V	1700 V	1200 V	1200 V	1200 V
$I_{DSS}$ at $T_j=25^\circ C$	100 $\mu A$	100 $\mu A$	60 $\mu A$	50 $\mu A$	100 $\mu A$	100 $\mu A$
$I_{DSS}$ at $T_j=135^\circ C$	-----	-----	-----	150 $\mu A$	250 $\mu A$	-----
$I_{DSS}$ at $T_j=150^\circ C$	-----	250 $\mu A$	120 $\mu A$	-----	-----	-----
$P(I_{DSS})$ at $T_j=25^\circ C$	0.12 W	0.12 W	0.102 W	0.06 W	0.12 W	0.12 W
$P(I_{DSS})$ at $T_j=135^\circ C$	-----	-----	-----	0.18 W	0.3 W	-----
$P(I_{DSS})$ at $T_j=150^\circ C$	-----	0.3 W	0.204 W	-----	-----	-----
$P_{tot}$	463 W	125 W	69 W	134 W	215 W	270 W

The analysis of this table shows that the dissipation resulting from leakage current  $I_{DSS}$  does not exceed 1% of the total wastes of the component.

### The thermal part model

The thermal impedance provided by the manufacturer’s datasheet represents the instantaneous increase in the junction temperature of the device as a function of time (Fig.7). It is represented by the RC pair of cells [22] [23], and is dependent on the size of the

semiconductor, the number and type of layers between the semiconductor and its case, and also the electrical insulation material. For our model we used 5 cells RC parallel. The values of  $R_i$  and  $C_i$  are derived from the datasheet curve, and calculated depending on  $Z_{th}$  values (column Y) and  $\tau_i$  (column X) for each  $n$  RC pairs according to equation (8).

$$Z_{Th}(t) = \sum_{i=1}^n R_i \left( 1 - \exp\left(-\frac{t}{\tau_i}\right) \right) \quad (8)$$

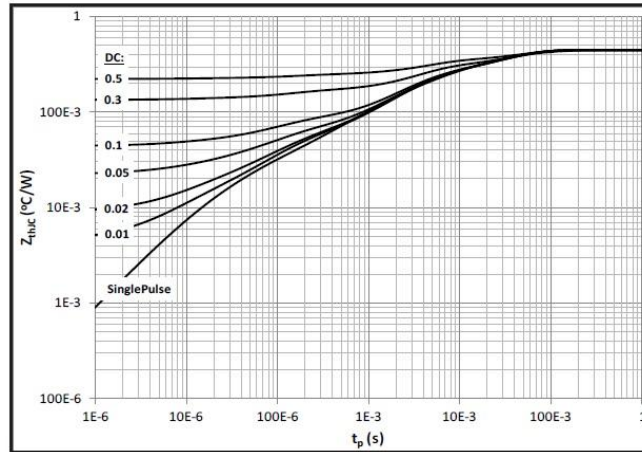


Fig.7: Typical Transient Thermal Impedance (Junction - Case) with Duty Cycle

We first determine  $Z_{Thmax}$  maximum value (in permanent state), and then the approximate values of the first pole position which are defined by  $Z_{Th}$  and its corresponding  $\tau$  (x-axis) (9). The remained values of  $R_n$  and  $\tau_n$  are respectively determined according to equations (10) and (11).

$$\tau_n = \frac{\tau_1}{n} \left( 0.1^{n-1} \right) \quad (9) \quad Z_{Th} = 0.7 \times Z_{Thmax} \quad (10)$$

$$R_n = R_1 \times 0.5^n \quad (11) \quad Erreur = \sum_1^i \left( \frac{R_\theta(i) - R_\theta(i)best}{R_\theta(i)best} \right)^2 \quad (12)$$

We use the Simulated Annealing (SA) [24], technique to browse randomly (starting from an initialization) the pair values  $Z_{th}$  and  $\tau$ . Then, we compare the error of the current iteration with the best error formerly found. The latter is calculated by the least squares (LS) method for each time step (12).

## RESULTS

To assess the accuracy of the proposed model described above, we performed simulations of some SiC MOSFET models. The model parameters (Table.2) are extracted and calculated by using Matlab software while adopting meanwhile mathematical methods: the simulated annealing (SA) and the weighted least squares (WLS).

TABLE II. Various model parameters for the six analyzed MOS transistors

		C2M0025120D	C2M0160120D	C2M1000170D	CMF10120D	CMF20120D	SCT30N120
<b>Thermal Parameters</b>							
<b>TR</b>	<b>TR1</b>	7.804e-02	7.164e-02	2.702e-01	2.967e-01	2.101e-01	2.784e-01
	<b>TR2</b>	3.294e-02	2.248e-01	8.317e-01	1.942e-01	1.740e-01	1.539e-01
	<b>TR3</b>	7.474e-03	1.949e-01	4.320e-01	2.915e-02	3.250e-02	4.216e-02
	<b>TR4</b>	1.199e-01	5.011e-01	1.753e-01	5.480e-03	2.327e-02	1.187e-02
<b>TC</b>	<b>TC1</b>	4.362e-01	1.222e+00	3.046e-01	2.926e-01	1.607e-01	1.640e-01
	<b>TC2</b>	7.776e-02	3.310e-02	8.842e-03	3.438e-02	1.960e-02	3.546e-02
	<b>TC3</b>	1.271e-02	5.082e-03	2.156e-03	1.098e-01	2.488e-03	1.077e-02
	<b>TC4</b>	3.275e-06	6.804e-07	1.781e-06	4.609e-05	1.821e-05	1.221e-03
<b>Input admittance</b>							
<b>Ga0</b>		-3.524e+02	-1.005e+02	-5.445e+00	0.000e+00	0.000e+00	0.000e+00
<b>Ga1</b>		7.343e-01	2.704e-01	-5.138e-02	-3.579e-01	-6.167e-01	-5.950e-01
<b>Ga2</b>		-4.267e-04	-2.112e-04	1.310e-04	6.985e-04	1.169e-03	9.045e-04
<b>Gb0</b>		3.367e+01	7.399e+00	-3.653e-01	0.000e+00	0.000e+00	0.000e+00
<b>Gb1</b>		-2.159e-02	-8.309e-03	1.095e-02	3.563e-02	6.647e-02	6.290e-02
<b>Gb2</b>		-1.041e-05	2.316e-06	-1.995e-05	-5.823e-05	-1.067e-04	-7.706e-05
<b>Dynamic capacitances</b>							
<b>C1</b>		1.052e-09	1.730e-10	2.147e-11	5.001e-10	1.072e-09	3.558e-10
<b>C2</b>		1.501e-11	4.045e-12	1.290e-12	7.341e-12	1.242e-11	2.849e-11
<b>C3</b>		2.738e-09	5.229e-10	1.281e-10	9.256e-10	1.902e-09	1.632e-09
<b>C6</b>		2.046e-10	4.310e-11	8.700e-12	5.536e-11	1.070e-10	1.170e-10
<b>VDSmax</b>		1.000e+03	1.000e+03	1.800e+03	8.000e+02	8.000e+02	1.000e+03
<b>Forward Conduction Voltage drop</b>							
<b>Ra0</b>		7.570e-02	-1.248e-01	1.541e-01	1.414e-01	-1.395e+00	-2.685e-01
<b>Ra1</b>		1.215e-04	8.101e-04	-3.832e-04	1.593e-04	5.333e-03	8.058e-04
<b>Rb0</b>		1.245e-03	6.035e-02	-5.590e-01	2.748e-02	1.336e-01	1.192e-01
<b>Rb1</b>		7.871e-05	2.605e-04	4.916e-03	2.565e-04	-2.589e-04	-8.979e-05
<b>Rc0</b>		-2.006e-04	-4.401e-03	9.177e-02	3.939e-03	-1.745e-03	1.915e-06
<b>Rc1</b>		1.210e-06	3.142e-05	3.907e-04	-5.650e-07	8.545e-06	1.425e-06

The findings of the calculations showed excellent agreement with the measured curves in the datasheets provided by the manufacturer in a wide range of operating temperatures. In this regard, the results of the transistor CMF20120D [20] are a good case in point as demonstrated below:

### MOS input admittance

The following figure (Fig.8) shows the evolution of  $I_D$  current as a function of  $V_{GS}$  for both temperatures (25°C and 135°C) and absolute error between the manufacturer's data and model of the MOS.

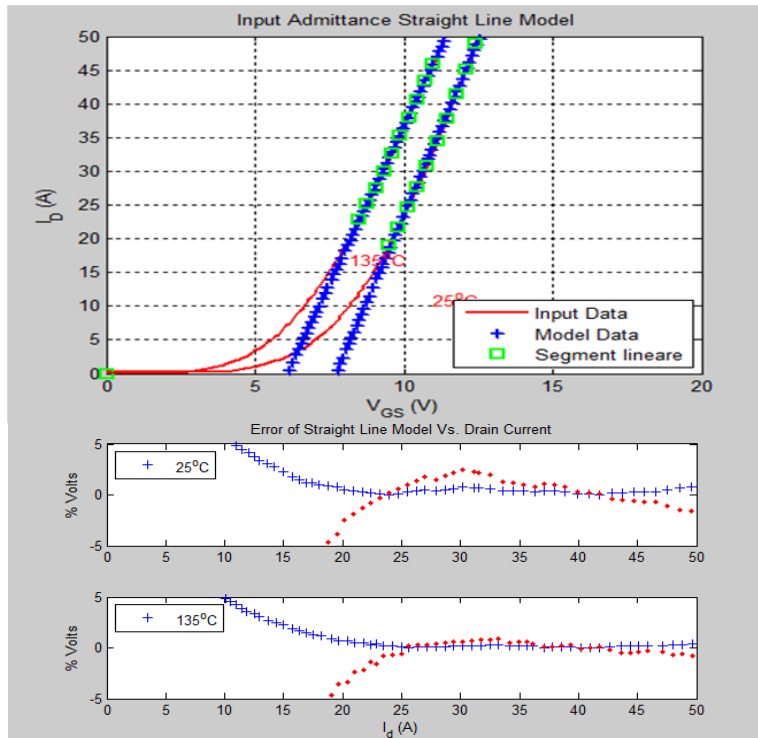


Fig.8: Input Data and Straight Line Model Input Admittance (above) and absolute error (bottom)

We can notice from the figure that the absolute error between the model and the manufacturer data does not exceed 5% starting from the 10A  $I_D$  current value but surpasses that percentage in lower value of  $I_D$  (<10A). But this affects in no way the accuracy of the model.

### MOS dynamic capacitances

The three capacitances of the MOS transistor variation versus time is shown in the following figure (Fig.9).

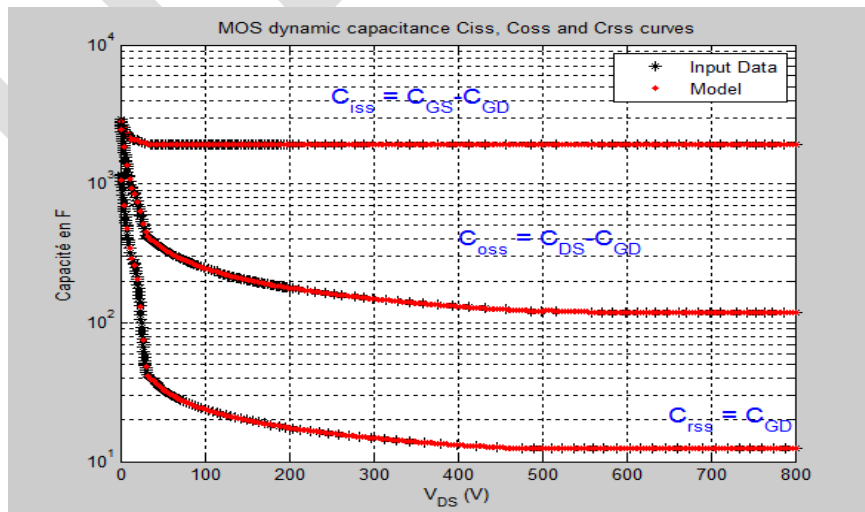


Fig 9 MOS dynamic capacitance  $C_{iss}$ ,  $C_{oss}$  and  $C_{rss}$  curves

We also note from the figure that the curves of the manufacturer's data and model fit perfectly over the entire band of  $V_{DS}$  variation. These results further confirm the usefulness of the proposed model.

### MOS forward Conduction Voltage drop

The curves in the figure (Fig.10) show the characteristics of the manufacturer data  $I_D(V_{DS})$  for  $V_{GS} = 16, 18$  and  $20V$ .

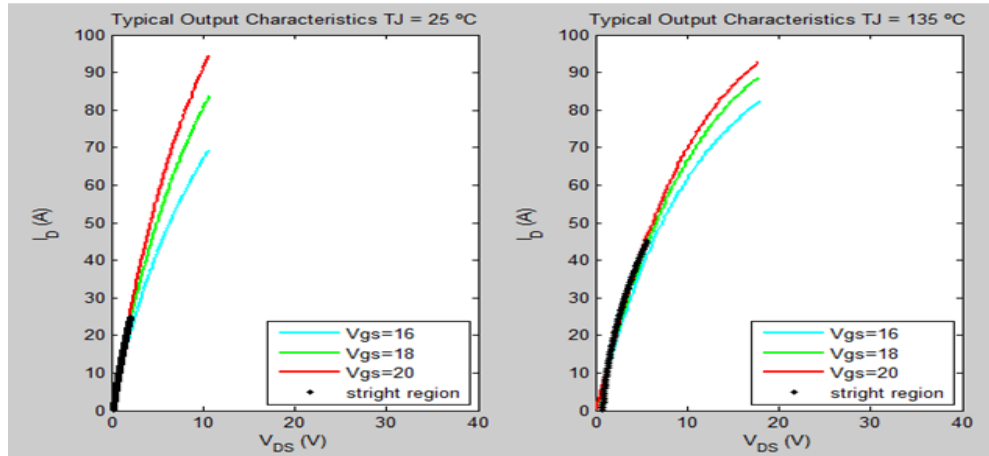


Fig 10 : Output characteristics as a function of gate voltage ( $V_{GS}=16V, 18V$  et  $20V$ ) for  $25^{\circ}C$  (left) and  $135^{\circ}C$  (right)

In this figure we notice an almost perfect correspondence between the curves of manufacturer's data and the straight-line of the model.

### MOS thermal impedance

The following figure (Fig.11) presents the evolution of the thermal impedance and its absolute error as generated over time.

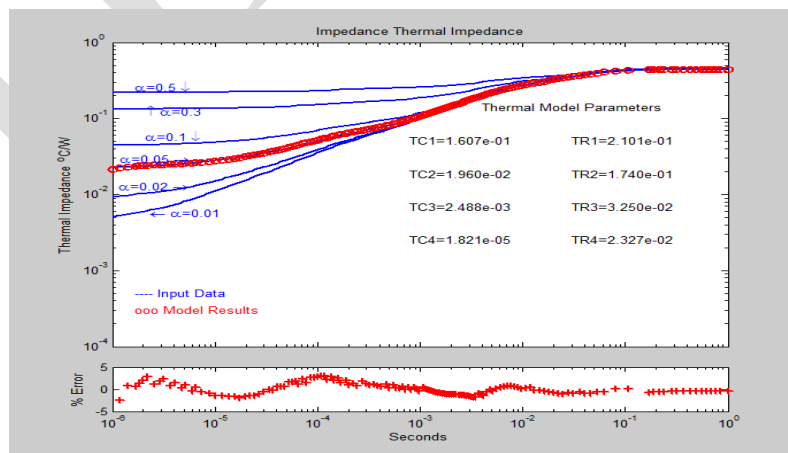


Fig 11 : Measured (Input data) and simulated thermal impedance characteristics

The curve clearly shows that the absolute error between the model and the manufacturer's data does not exceed 3%. This low value allows us to suffice with four cells of the (RC) Foster network for the representation of the thermal impedance. Consequently the thermal effect was taken into account using only a small number of cells which in effect reduces the complexity of the proposed model.

## CONCLUSION

This behavioral electro-thermal model of the MOS transistor SiC showed perfect agreement with the manufacturer's data. The parameters estimating procedure which is based on Least Square Balanced (WLS) and simulated annealing (SA) methods has yielded up good results (the error margin does not exceed 5%). The advantages of this model lie in its simplicity, flexibility and feasibility as to be implemented in on Spice-based modern simulators such as BSIM, PSPICE, LTSpice and OrCAD Spice. However; it is still in a process of development with regard to modeling the quasi-saturation and input admittance.

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