

## MODELING AND ANALYSIS OF DSTATCOM FOR REACTIVE POWER IMPROVEMENT AND HARMONICS REDUCTION IN POWER SYSTEM

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**Abstract-** Distribution static compensator (DSTAT COM) is a shunt compensation device that is generally used to solve power quality problems in distribution systems. In an all-electric ship power system, power quality issues arise due to high-energy demand loads such as pulse loads. In this paper a new algorithm to generate reference voltage for a distribution static compensator (DSTATCOM) operating in voltage-control mode. The magnitude of the bus voltage is chosen as nominal value, i.e., 1.0 p.u., while its phase angle is obtained through a feedback loop that maintains the voltage across the DC storage capacitors. The proposed scheme ensures that unity power factor (UPF) is achieved at the load terminal during nominal operation, which is not possible in the traditional method. DSTAT COM to tackle power-quality issues by providing power factor correction, harmonic elimination, load balancing, and voltage regulation based on the load requirement and simulation results are presented by using Matlab/ simulink platform.

**Index Terms—** Current control mode, power quality (PQ), voltage-control mode, voltage-source inverter.

### I. INTRODUCTION

In power distribution networks, reactive power is the main cause of increasing distribution system loss and various power quality problems. Conventionally, static Var compensator (SVCs) have been used in conjunction with passive filters at the distribution level for reactive power compensation and mitigation of power quality problems. Though SVCs are very effective system controllers used to provide reactive power compensation at the transmission level, their limited bandwidth, higher passive element count that increases size and losses, and slower response make them inapt for the modern day distribution requirement. Another compensating system has been proposed by, employing a combination of SVC and active power filter, which can compensate three phase loads in a minimum of two cycles. Thus, a controller which continuously monitors the load voltages and currents to determine the right amount of compensation required by the system and the less response time should be a viable alternative. Distribution Static compensator (DSTATCOM) has the capacity to overcome the above mentioned drawbacks by providing precise control and fast response during transient and steady state, with reduced footprint and weight. A DSTATCOM is basically a converter based distribution flexible AC transmission controller, sharing many similar concepts with that of a Static Compensator (STATCOM) used at the transmission level. At the transmission level, STATCOM handles only fundamental reactive power and provides voltage support, while a DSTATCOM is

employed at the distribution level or at the load end for dynamic compensation. The latter, DSTATCOM, can be one of the viable alternatives to SVC in a distribution network. Additionally, a DSTATCOM can also behave as a shunt active filter, to eliminate unbalance or distortions in the source current or the supply voltage, as per the IEEE-519 standard limits. Since a DSTATCOM is such a multifunctional device, the main objective of any control algorithm should be to make it flexible and easy to implement, in addition to exploiting its multi functionality to the maximum. Prior to the type of control algorithm incorporated, the choice of converter configuration is an important criterion. The two converter configurations are voltage source converter or current source converter, in addition to passive storage elements, either a capacitor or an inductor respectively. Normally, voltage source converters are preferred due to their smaller size, less heat dissipation and less cost of the capacitor, as compared to an inductor for the same rating. This paper focuses on the comparative study of the control techniques or voltage reactive power compensation, and voltage supports and are recently being incorporated to a control a DSTATCOM employed at the distribution end. The following indices are considered for comparison measurement an signal conditioning requirements, performance with varying linear/nonlinear load, total harmonic distortion (THD), DC link voltage variation and switching frequency. The paper briefly describes the salient features of each strategy, with their merits and demerits. The paper also emphasizes the choice of current control technique, as it significantly affects the performance of a DSTATCOM. A dynamic simulation model of the DSTATCOM has been developed for various control algorithms in Matlab / Sim Power System environment.

## II. PROPOSED CONTROL SCHEME

Circuit diagram of a DSTATCOM-compensated distribution system is shown in Fig. 1. It uses a three-phase, four-wire, two-level, neutral-point-clamped VSI. This structure allows independent control to each leg of the VSI [7]. Fig. 2 shows the single-phase equivalent representation of Fig. 1. Variable is a switching function, and can be either +1 or -1 depending upon switching state. Filter inductance and resistance  $L_f$  are  $R_f$  and , respectively. Shunt capacitor  $C_{fc}$  eliminates high-switching frequency components. First, discrete modeling of the system is presented to obtain a discrete voltage control law, and it is shown that the PCC voltage can be regulated to the desired value with properly chosen parameters of the VSI. Then, a procedure to design VSI parameters is presented. A proportional-integral (PI) controller is used to regulate the dc capacitor voltage at a reference value.

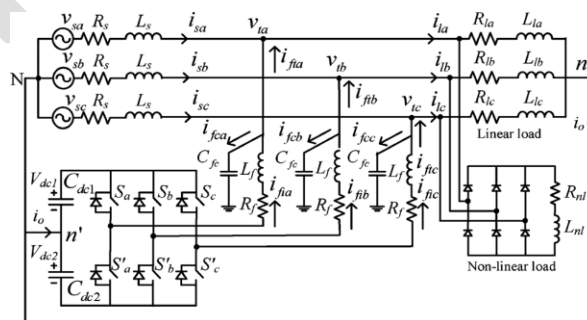


Fig. 1. Circuit diagram of the DSTATCOM- compensated distribution system.

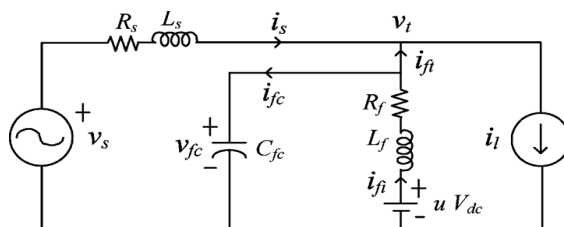


Fig.2.Single-phase equivalent circuit of DSTATCOM.

Based on instantaneous symmetrical component theory and complex Fourier transform, a reference voltage magnitude generation scheme is proposed that provides the advantages of CCM at nominal load. The overall controller block diagram is shown in Fig. 3. These steps are explained as follows.

### A System Modeling and Generation of the Voltage-Control Law

The state-space equations for the circuit shown in Fig. 2 are given by

$$\dot{x} = Ax + Bz \quad (1)$$

Where

$$A = \begin{bmatrix} 0 & \frac{1}{C_{fc}} & 0 \\ -\frac{1}{L_f} & -\frac{R_f}{L_f} & 0 \\ -\frac{1}{L_s} & 0 & \frac{R_s}{L_s} \end{bmatrix}, \quad B = \begin{bmatrix} 0 & -\frac{1}{C_{fc}} & 0 \\ -\frac{V_{dc}}{L_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L_s} \end{bmatrix},$$

$$X = [V_{fc} \ i_{fi} \ i_s]^t, \quad z = [u \ i_{ft} \ v_s]^t$$

The general time-domain solution of (1) to compute the state vector  $x(t)$  with known initial value  $x(t)_0$ , is given as follows

$$x(t) = e^{A(t-t_0)}x(t_0) + \int_{t_0}^t e^{A(t-\tau)} Bz(\tau)d\tau \quad (2)$$

The equivalent discrete solution of the continuous state is obtained by replacing  $t_0 = kT_d$  and  $t = (k+1)T_d$  as follows

$$x(k+1) = e^{AT_d}x(k) + \int_{kT_d}^{T_d+kT_d} e^{A(T_d+kT_d-\tau)} Bz(\tau)d\tau \quad (3)$$

In (3),  $k$  and  $T_d$  represent the  $k$ th sample and sampling period, respectively. During the consecutive sampling period, the value of  $z(\tau)$  is held constant, and can be taken as  $z(k)$ . After simplification and changing the integration variable, (3) is written as [18]

$$x(k+1) = e^{AT_d}x(k) + \int_0^{T_d} e^{A\lambda}Bd\lambda z(k) \quad (4)$$

Equation (4) is rewritten as follows

$$x(k+1) = Gx(k) + Hz(k) \quad (5)$$

Where  $G$  and  $H$  are sampled matrices, with a sampling time of  $T_d$ . For small sampling time, matrices  $G$  and  $H$  are calculated as follows

$$G = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} = e^{AT_d} \approx I + AT_d + \frac{A^2T_d^2}{2} \quad (6)$$

$$H = \begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} = \int_0^{T_d} e^{A\lambda}Bd\lambda \approx \int_0^{T_d} (I + A\lambda)Bd\lambda \quad (7)$$

From (6) and (7)  $G_{11} = 1 - \frac{T_d^2}{2L_f C_{fc}}$ ,  $G_{12} = \frac{T_d}{C_{fc}} - \frac{T_d^2 R_f}{2L_f C_{fc}}$ ,  $G_{13} = 0$

$H_{11} = \frac{T_d^2 V_{dc}}{2L_f C_{fc}}$ ,  $H_{12} = -\frac{T_d}{C_{fc}}$ , and  $H_{13} = 0$

hence, the capacitor voltage using (5) is given as

$$v_{fc}(k+1) = G_{11}v_{fc}(k) + G_{12}i_{fi}(k) + H_{11}u(k) + H_{12}i_{ft}(k) \quad (8)$$

As seen from (8), the terminal voltage can be maintained at a reference value depending upon the VSI parameters, , , , and sampling time  $T_d$ . Therefore, VSI parameters  $V_{dc}$ ,  $C_{fc}$ ,  $R_f$ ,  $L_f$  must be chosen carefully. Let  $V_t^*$  be the reference load terminal voltage. A cost function is chosen as follows [8]:

$$J = [v_{fc}(k+1) - V_t^*(k+1)]^2 \quad (9)$$

The cost function is differentiated with respect to  $u(k)$  and its minimum is obtained

$$v_{fc}(k+1) = V_t^*(k+1) \quad (10)$$

The deadbeat voltage-control law, from (8) and (10), is given as

$$u^*(k) = \frac{V_t^*(k+1) - G_{11}v_{fc}(k) - G_{12}i_{fi}(k) - H_{12}i_{ft}(k)}{H_{11}} \quad (11)$$

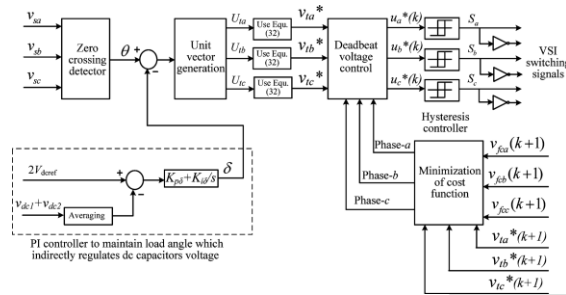


Fig. 3. Overall block diagram of the controller to control DSTATCOM in a distribution system.

In (11),  $V_t^*(k+1)$  is the future reference voltage which is unknown. One-step-ahead prediction of this voltage is done using a second-order Lagrange extrapolation formula as follows

$$V_t^*(k+1) = 3V_t^*(k-1) + V_t^*(k-2) \quad (12)$$

The term  $V_t^*(k+1)$  is valid for a wide frequency range [17] and when substituted in (11), yields to a one-step-ahead deadbeat voltage-control law. Finally  $u^*(k)$ , is converted into the ON/OFF switching command to the corresponding VSI switches using a deadbeat hysteresis controller [17].

#### A. Design of VSI Parameters

DSTATCOM regulates terminal voltage satisfactorily, depending upon the properly chosen VSI parameters. The design procedure of these parameters is presented as follows.

1) *Voltage Across DC Bus ( $V_{dc}$ )* : The dc bus voltage is taken twice the peak of the phase voltage of the source for satisfactory performance [19]. Therefore, for a line voltage of 400 V, the dc bus voltage is maintained at 650 V.

2) *DC Capacitance ( $C_{dc}$ )* : Values of dc capacitors are chosen based on a period of sag/swell and change in dc bus voltage during transients. Let the total load rating be SkVA. In the worst case, the load power may vary from minimum to maximum that is, from 0 to S kVA. The compensator needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in the deviation of capacitor voltage from its reference value. The voltage continues to decrease until the capacitor voltage controller comes into action. Consider that the voltage controller takes  $p^T$  cycles, that is, seconds to act, where T is the system time period. Hence, maximum energy exchange by the compensator during transient will be . This energy will be  $p^{ST}$  equal to the change in the capacitor stored energy. Therefore

$$\frac{1}{2}C_{dc}(V_{dc}^2 - V_{dc}^2) = p^{ST} \quad (13)$$

Where  $V_{dcref}$  and  $V_{dc}$  are the reference dc bus voltage and maximum-allowed voltage during transients, respectively. Hence

$$C_{dc} = \frac{2p^{ST}}{V_{dcref}^2 - V_{dc}^2} \quad (14)$$

Here,  $S=10$  kVA,  $V_{dcref} = 650$  V,  $p = 1$ , and  $V_{dc} = 0.8V_{dcref}$  or  $1.2V_{dcref}$ . Using (14), capacitor values are found to be  $2630 \mu F$  and  $2152 \mu F$ . The capacitor value 2600 is chosen to achieve satisfactory performance during all operating conditions.

3) *Filter Inductance ( $L_f$ )* : Filter inductance  $L_f$  should provide reasonably high switching frequency and a sufficient rate of change of current such that VSI currents follow desired currents. The following equation represents inductor dynamics

$$L_f \frac{di_{fi}}{dt} = -V_{fc} - R_f i_{fi} + V_{dc} \quad (15)$$

The inductance  $L_f$  is designed to provide good tracking performance at a maximum switching frequency ( $f_{max}$ ) which is achieved at the zero of the source voltage in the hysteresis controller. Neglecting  $R_f$ ,  $L_f$  is given by

$$L_f = \frac{2V_m}{(2h_c)(2f_{max})} = \frac{0.5V_m}{h_c 2f_{max}} \quad (16)$$

Where  $2h_c$  is the ripple in the current. With  $f_{max} = 10$  kHz and  $h_c = 0.75$  A (5% of rated current), the value of  $L_f$  using (16) is found to be 21.8 mH, and 22 mH is used in realizing the filter.

4) *Shunt Capacitor ( $C_{fc}$ )* : The shunt capacitor should not resonate with feeder inductance at the fundamental frequency ( $\omega$ ). Capacitance, at which resonance will occur, is given as (17)

$$C_{fcr} = \frac{1}{\omega_0^2 L_s} \quad (17)$$

For proper operation,  $C_{fc}$  must be chosen very small compared to  $C_{fcr}$ . Here, a value of 5 F is chosen which provides an impedance of  $637 \Omega$  at  $\omega_0$ . This does not allow the capacitor to draw significant fundamental reactive current.

$$P_{pcc} = P_{avg} + P_{loss} \quad (18)$$

### C. Controller for DC Bus Capacitor Voltage

Average real power balance at the PCC will be

$$\delta = k_{i\delta} e_{vdc} + K_{i\delta} \int e_{vdc} dt \quad (19)$$

where,  $P_{pcc}$ ,  $P_{avg}$  and  $P_{loss}$ , are the average PCC power, load power, and losses in the VSI, respectively. The power available at the PCC, which is taken from the source, depends upon the angle between source and PCC voltages, that is, load angle. Hence, must be maintained constant to keep constant  $P_{pcc}$ . The voltage of the dc bus of DSTATCOM can be maintained at its reference value by taking inverter losses  $P_{loss}$ , from the source. If the capacitor voltage is regulated to a constant reference value  $P_{loss}$ , is a constant value. Consequently, is also a constant value. Thus, it is evident that dc-link voltage can be regulated by generating a suitable value of  $\delta$ . This includes the effect of losses in the VSI and, therefore, it takes care of the term  $P_{loss}$ , in its

action. To calculate load angle, the averaged dc-link voltage ( $V_{dc1} + V_{dc2}$ ) is compared with a reference voltage, and error is passed through a PI controller. The output of the PI controller, which is load angle, is given as follows

Where  $e_{vdc} = 2V_{dcref} - (V_{dc1} + V_{dc2})$  is the voltage error. Terms  $k_{p\delta}$  and  $k_{i\delta}$  are proportional and integral gains, respectively.  $\delta$  must lie between 0 to 90 for the power flow from the source to PCC. Hence, controller gains must be chosen carefully.

#### A. Proposed Method To Generate Reference Terminal Voltages

Reference terminal voltages are generated such that, at nominal load, all advantages of CCM operation are achieved while DSTATCOM is operating in VCM. Hence, the DSTATCOM will inject reactive and harmonic components of load current. To achieve this, first the fundamental positive-sequence component of load currents is computed. Then, it is assumed that these currents come from the source and considered as reference source currents at nominal load. With these source currents and for UPF at the PCC, the magnitude of the PCC voltage is calculated. Let three-phase load currents  $i_{la}(t)$ ,  $i_{lb}(t)$  and  $i_{lc}(t)$  be represented by the following equations:

$$i_{ij}(t) = \sum_{n=1}^m \sqrt{2} I_{ijn} \sin(n\omega t + \phi_{ijn}) \quad (20)$$

Where  $j=a,b,c$  represent three phases,  $n$  is the harmonic number, and  $m$  is the maximum harmonic order  $\phi_{lan}$  represents the phase angle of the  $n$ th harmonic with respect to reference in phase- and is similar to other phases. Using instantaneous symmetrical component theory, instantaneous zero-sequence  $i_{la}^0(t)$ , positive-sequence  $i_{la}^+(t)$ , and negative-sequence  $i_{la}^-(t)$  current components are calculated as follows

$$\begin{bmatrix} i_{la}^0(t) \\ i_{la}^+(t) \\ i_{la}^-(t) \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} i_{la}(t) \\ i_{lb}(t) \\ i_{lc}(t) \end{bmatrix} \quad (21)$$

Where  $\alpha$  is a complex operator and defined by  $e^{j2\pi/3}$

The fundamental positive-sequence component  $i_{la1}^+(t)$  of load current, calculated by finding the complex Fourier coefficient, is expressed as follows

$$\bar{I}_{la1}^+ = \frac{\sqrt{2}}{T} \int_0^T i_{la}^+(t) e^{-j(\omega t - 90^\circ)} dt \quad (22)$$

$\bar{I}_{la1}^+$  is a complex quantity, contains magnitude and phase angle information, and can be expressed in phasor form as follows:

$$\bar{I}_{la1}^+ = |\bar{I}_{la1}^+| \angle \bar{I}_{la1}^+ \quad (23)$$

Hence, the instantaneous fundamental positive-sequence component of load current in phase-,  $i_{la}^+(t)$ , is expressed as

$$i_{la}^+(t) = \sqrt{2} |\bar{I}_{la1}^+| \sin(\omega t + \angle \bar{I}_{la1}^+) \quad (24)$$

The fundamental positive-sequence component of load currents must be supplied by the source at nominal load. Hence, it will be treated as reference source currents. For UPF at nominal operation, the nominal load angle  $\delta_0$  is used. By knowing  $i_{la1}^+(t)$ , fundamental positive-sequence

currents in phases and can be easily computed by providing a phase displacement of  $-\frac{2\pi}{3}$  and  $+\frac{2\pi}{3}$ , respectively, and are given as

$$\begin{aligned} i_{sa}^* &= i_{la1}^+(t) = \sqrt{2}|\bar{I}_{la1}^+| \sin(\omega t - \delta_0) \\ i_{sb}^* &= i_{lb1}^+(t) = \sqrt{2}|\bar{I}_{la1}^+| \sin(\omega t - \frac{2\pi}{3} - \delta_0) \\ i_{sc}^* &= i_{lc1}^+(t) = \sqrt{2}|\bar{I}_{la1}^+| \sin(\omega t + \frac{2\pi}{3} - \delta_0) \end{aligned} \quad (25)$$

When reference source currents derived in (25) are supplied by the source, three-phase terminal voltages can be computed using the following equations:

$$v_{tj}(t) = v_{sj}(t) - L_s \frac{di_{sj}^*}{dt} - R_s i_{sj}^* \quad (26)$$

Let the rms value of reference terminal and source voltages be  $V_t^*$  and  $V$ , respectively. For UPF, the source current and terminal voltage will be in phase. However, to obtain the expression of independent of  $V^*$ , we assume the PCC voltage as a reference phasor for the time-being. Hence, phase- quantities, by considering UPF at the PCC, will be Substituting (27) into (26), the phasor equation will be Simplifying the equation (28)

$$\begin{aligned} v_{ta}(t) &= \sqrt{2}v_t^* \sin \omega t \\ i_{sa}^* &= \sqrt{2}|\bar{I}_{la1}^+| \sin \omega t \\ v_{sa}(t) &= \sqrt{2}V \sin(\omega t + \delta_0) \end{aligned} \quad (27)$$

$$V_t^* L_0 = VL\delta_0 - (R_s + jX_s)|\bar{I}_{la1}^+|L_0 \quad (28)$$

$$V_t^* = V \cos \delta_0 + j \sin \delta_0 - |\bar{I}_{la1}^+|R_s - j|\bar{I}_{la1}^+|X_s \quad (29)$$

Equating real and imaginary parts of both sides of (29), the following equation is obtained:

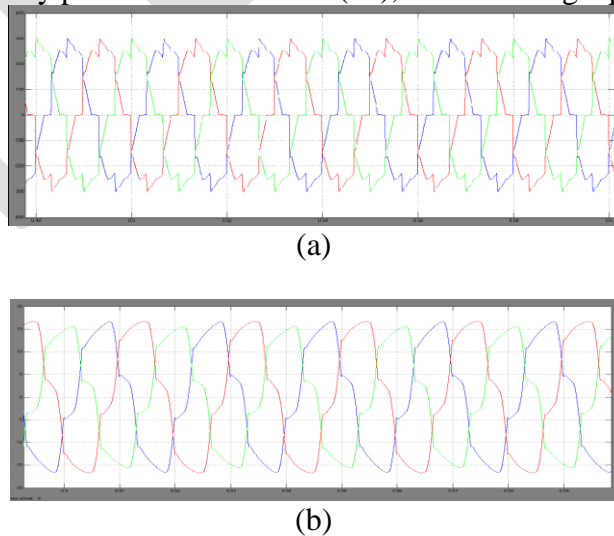


Fig. 4. Before compensation. (a) Terminal voltages. (b) Source currents

To remove  $\delta_0$  from (30), both sides are squared and added to obtain the following:

$$\begin{aligned} V \cos \delta_0 &= V_t^* + |\bar{I}_{la-1}^+| R_s \\ V \sin \delta_0 &= |\bar{I}_{la-1}^+| X_s \end{aligned} \quad (30)$$

$$V^2 = (V_t^* + |\bar{I}_{la-1}^+| R_s)^2 + (|\bar{I}_{la-1}^+| X_s)^2 \quad (31)$$

After rearranging (31), the expression for reference load voltage magnitude will be

$$V_t^* = \sqrt{V^2 - (|\bar{I}_{la-1}^+| X_s)^2} - |\bar{I}_{la-1}^+| R_s \quad (32)$$

Finally, using  $V_t^*$  from (32), the load angle from (19), and the phase- source voltage as reference, three-phase reference terminal voltages are given as

$$\begin{aligned} v_{la}^*(t) &= \sqrt{2} V_t^* \sin(\omega t - \delta) \\ v_{lb}^*(t) &= \sqrt{2} V_t^* \sin(\omega t - \frac{2\pi}{3} - \delta) \\ v_{lc}^*(t) &= \sqrt{2} V_t^* \sin(\omega t + \frac{2\pi}{3} - \delta) \end{aligned} \quad (33)$$

### III. SIMULATION RESULTS

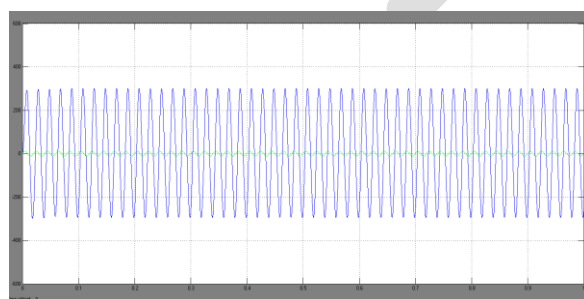
The control scheme is implemented using PSCAD software. Simulation parameters are given in Table I. Terminal voltages and source currents before compensation are plotted in Fig. 4. Distorted and unbalanced source currents flowing through the feeder make terminal voltages unbalanced and distorted. Three conditions, namely, nominal operation, operation during sag, and operation during load change are compared between the traditional and proposed method. In the traditional method, the reference voltage is 1.0 p.u. [2], [8]–[11], whereas in the proposed method, (32) is used to find the reference voltage.

#### A. Nominal Operation

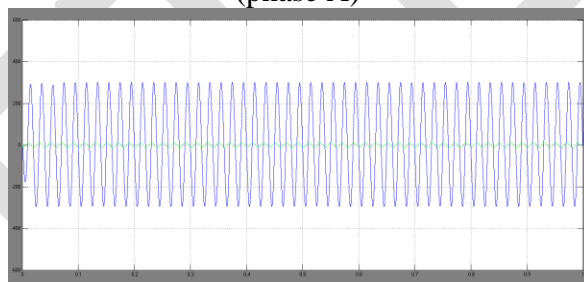
Initially, the traditional method is considered. Fig. 5(a)–(c) shows the regulated terminal voltages and corresponding source currents in phases, and, respectively. These waveforms are balanced and sinusoidal. However, source currents lead respective terminal voltages which show that the compensator supplies reactive current to the source to overcome feeder drop, in addition to supplying load reactive and harmonic currents. Fig. 6(a)

TABLE I  
SIMULATION PARAMETERS

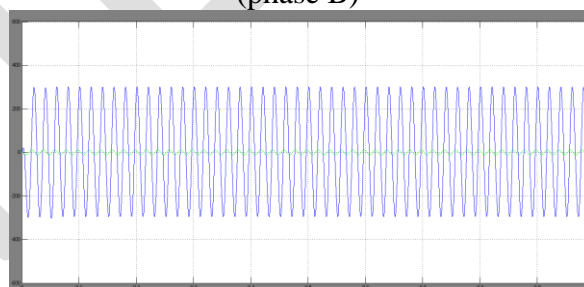
System quantities	Values
Source voltage	400 V rms line to line, 50 Hz
Feeder impedance	$Z_s = 1 + j3.14 \Omega$
Linear load	$Z_{la} = 30 + j62.8 \Omega$ , $Z_{lb} = 40 + j78.5 \Omega$ , $Z_{lc} = 50 + j50.24 \Omega$
Non-linear load	An R-L load of $50 + j62.8 \Omega$
VSI parameters	$V_{dc} = 650 \text{ V}$ , $C_{dc} = 2600 \mu\text{F}$ , $R_f = 1 \Omega$ , $L_f = 22 \text{ mH}$ , $C_{fc} = 5 \mu\text{F}$ , $I_{rated} = 30 \text{ A}$
PI gains	$K_{p\delta} = 8.5 e^{-7}$ , $K_{i\delta} = 1.8 e^{-6}$
Hysteresis band ( $h$ )	1 V



(phase A)



(phase B)



(phase C)

Fig. 5. Terminal voltages and source currents using the traditional method. (a) Phase- . (b) Phase- . (c) Phase- c

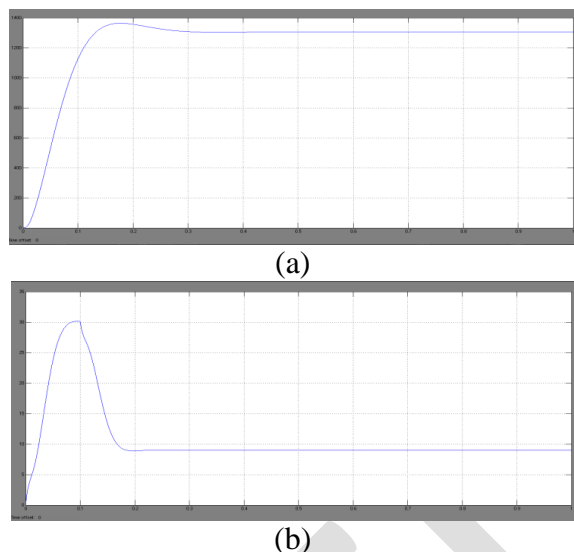


Fig. 6. (a) Voltage at the dc bus. (b) Load angle.

shows the dc bus voltage regulated at a nominal voltage of 1300 V. Fig. 6(b) shows the load angle settled around 8.50. Using the proposed method, terminal voltages and source currents in phases , , and are shown in Fig. 7(a)–(c), respectively. It can be seen that the respective terminal voltages and source currents are in phase with each other, in addition to being balanced and sinusoidal. Therefore, UPF is achieved at the load terminal. For the considered system, waveforms of load reactive power ( $Q_{Load}$ ), compensator reactive power ( $Q_{VSI}$ ), and reactive power at the PCC ( $Q_{PCC}$ ) in the traditional and proposed.

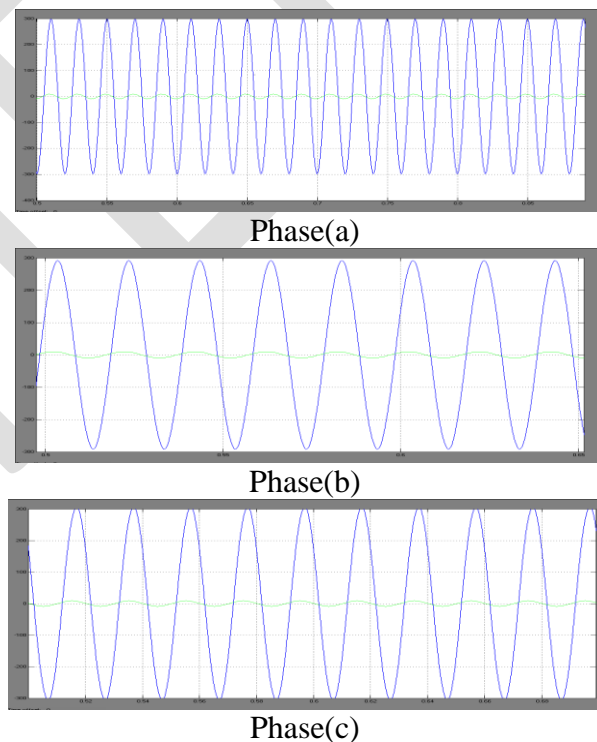


Fig. 7. Terminal voltages and source currents using the proposed method. (a) Phase- . (b) Phase- . (c) Phase-c .

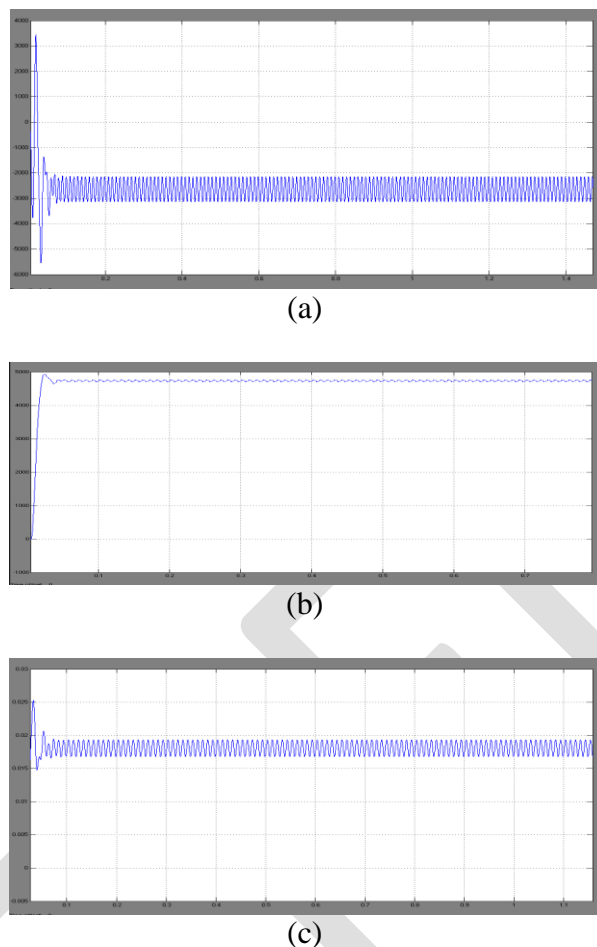


Fig. 8. Load reactive power ( $Q_{VSI}$ ), compensator reactive power ( $Q_{Load}$ ), and reactive power at PCC ( $Q_{PCC}$ ). (a) Traditional method. (b) Proposed method.

methods are given in Fig. 8(a) and (b), respectively. In the traditional method, the compensator needs to overcome voltage drop across the feeder by supplying reactive power into the source. As shown in Fig. 8(a), reactive power that is supplied by the compensator and has a value of 4.7 kVAr is significantly more than the load reactive power demand of 2.8 kVAr. This additional reactive power of 1.9 kVAr goes into the source. This confirms that significant reactive current flows along the feeder in the traditional method. However, in the proposed method, UPF is achieved at the PCC by maintaining suitable voltage magnitude. Thus, the reactive power supplied by the compensator is the same as that of the load reactive power demand. Consequently, reactive power exchanged by the source at the PCC is zero. These waveforms are given in Fig. 8(b). Fig. 9(a) and (b) shows the source rms currents in phase for the traditional and proposed methods, respectively. The source current has decreased from 11.35 to 10.5 A in the proposed method. Consequently, it reduces the ohmic losses in the feeder. Fig. 10(a) and (b) shows the compensator rms currents in phase- for the traditional and proposed methods, respectively. The current has decreased from 8.4 to 5.2 A in

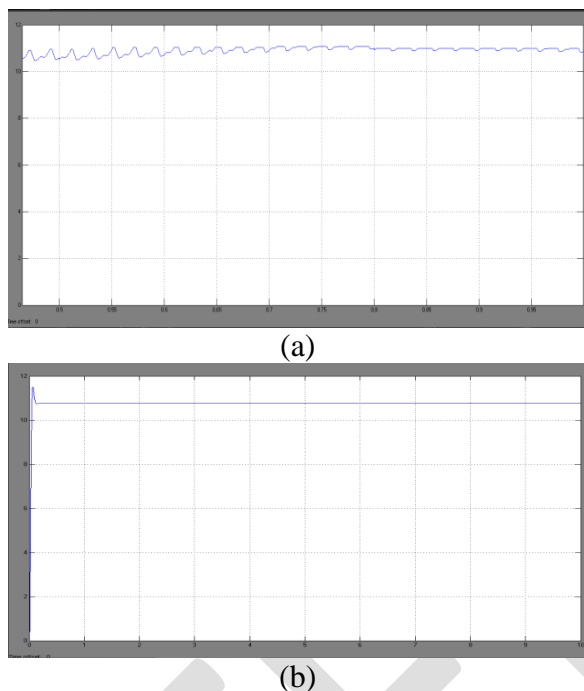


Fig. 9. Phase- source rms currents. (a) Traditional method. (b) Proposed method.

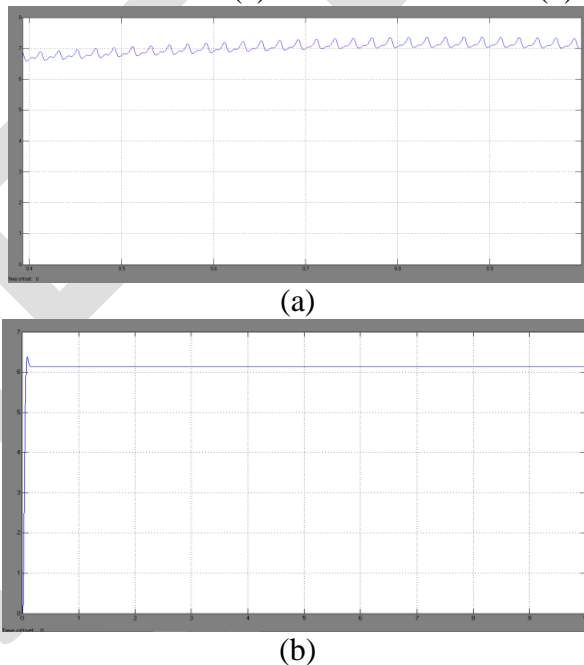


Fig. 10. Phase- compensator rms currents. (a) Traditional method. (b) Proposed method the proposed method. Losses in the VSI ( $P_{loss}$ ) represented by resistance ( $R_f$ ), and rating of VSI ( $S_{VSI}$ ) are defined as follows:

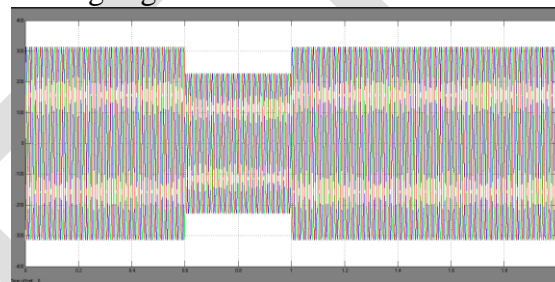
$$P_{loss} = 3I_{fi}^2 R_f \quad (34)$$

$$S_{VSI} = \sqrt{3} \frac{V_{dc}}{\sqrt{2}} I_{fi} \quad (35)$$

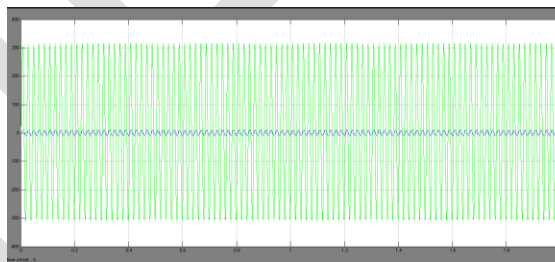
Using (34) and (35), VSI losses are reduced by 61.68% and only 61.9% VSI rating is utilized in the proposed method. In the traditional method, DSTATCOM maintains a load terminal voltage at 1.0 p.u. For this, it needs to compensate for the entire feeder drop. Hence, at the steady state, the compensator supplies reactive power to the source to overcome this drop. However, in the proposed scheme, the compensator does not compensate for the feeder drop in the steady-state condition. Hence, a lesser rating of VSI is utilized in the steady state. This savings in rating is utilized to mitigate deep sag, and DSTATCOM capacity to mitigate deep sag increases.

### *B. Operation During Sag*

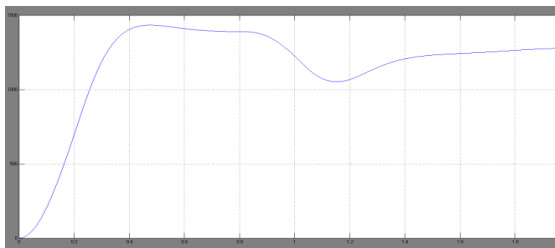
To create sag, source voltage is lowered by 20% from its nominal value at  $t = 0.6$  s as shown in Fig. 11(a). Sag is removed at  $t = 1.0$  s as shown in Fig. 11(b). Since voltage regulation capability does not depend upon reference voltage, it is not shown separately for the traditional method. Fig. 11(c) and (d) shows terminal voltages regulated at their reference value. The controller provides a fast voltage regulation at the load terminal. Fig. 11(e) and (f) shows the total dc bus voltage and the load angle, respectively. During the transient period, capacitors supply real power to maintain load power which results in discharging of capacitors. Consequently, increases to draw more power from the source compared to normal operation. After some time, the dc bus voltage again reaches



(a)&(b)



(c)&(d)



(e)

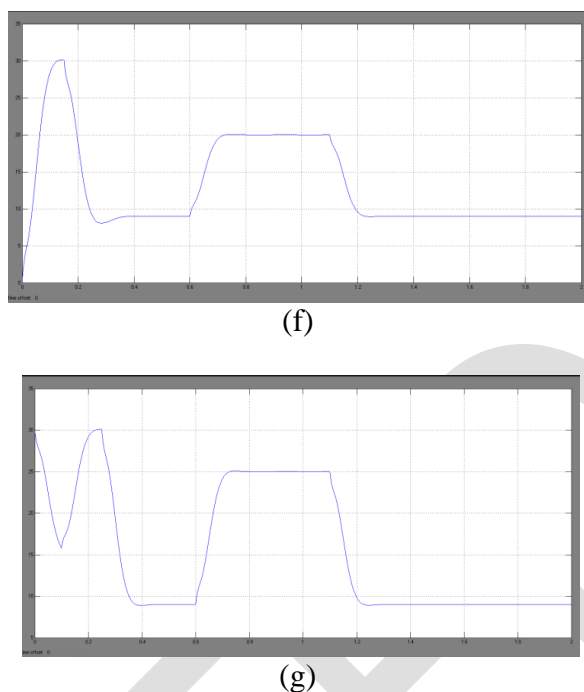


Fig. 11. (a) Source voltages during normal to sag. (b) Source voltages during sag to normal. (c) Terminal voltages during normal to sag. (d) Terminal voltages during sag to normal. (e) Voltage at the dc bus. (f) Load angle. (g) Compensator rms current in the traditional method. (h) Compensator rms current in the proposed method. the reference voltage whereas the load angle settles down at 17.4°.

However, the load angle again settles down at nominal value once the sag gets cleared. Compensator rms currents in the traditional and proposed method in phase- are shown in Fig. 11(g) and (h), respectively. In the proposed method, compensator rms current has decreased to 21.3 from 24.8 A. Loss reduction and percentage loss reduction in the VSI are given as.

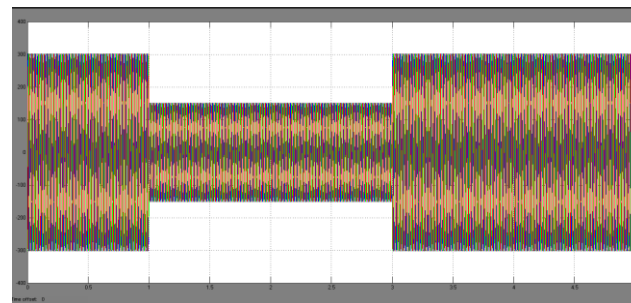
$$\Delta p_{loss} = 3(24.8^2 - 21.3^2)I = 484W$$

$$\frac{\Delta p_{loss}}{p_{loss}} = \frac{24.8^2 - 21.3^2}{24.8^2} = -26.23\%$$

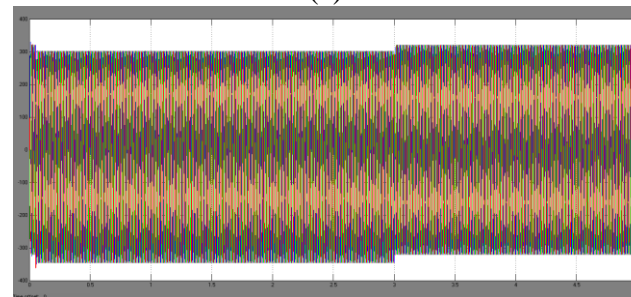
Also, savings in utilization of the VSI rating will be

$$\Delta S_{vsi} = \sqrt{3} \frac{650}{\sqrt{2}} (24.8 - 21.3) = 2790 VA.$$

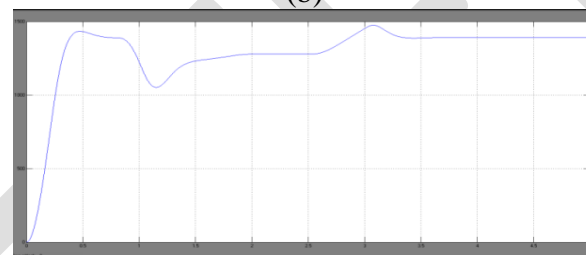
If the rating of VSI is limited to mitigate 20% sag, then this savings in rating can be used to mitigate additional sag. To show the capability of DSTATCOM to mitigate deep sag for a longer time, the source voltage is decreased to 60% of the nominal value for  $t = 1$  to 3 s duration as shown in Fig. 12(a).



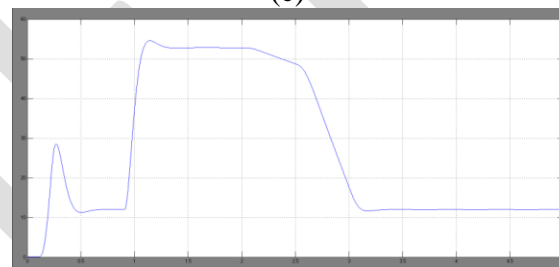
(a)



(b)

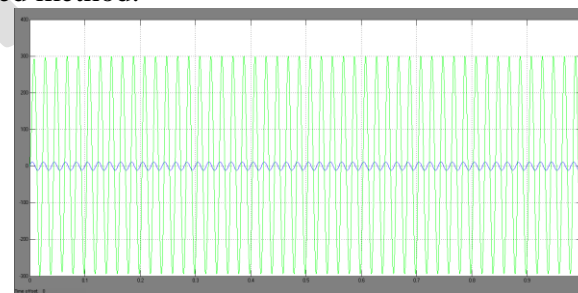


(c)

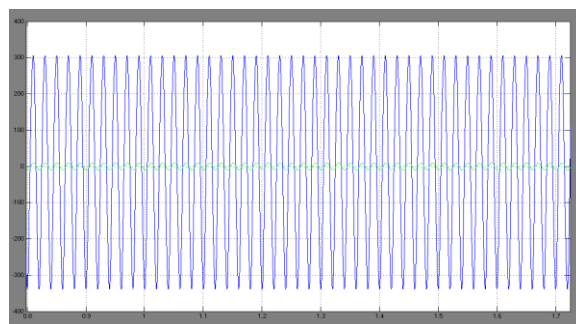


(d)

Fig. 12. (a) Source voltages. (b) Terminal voltages. (c) Voltage at the dc bus. (d) Compensator rms current in the proposed method.



(a)



(b)

Fig. 13. Terminal voltage and source current in phase- during load change.(a) Traditional method. (b) Proposed method.

The terminal voltages, maintained at the reference value, are shown in Fig. 12(b). The voltage across the dc bus is shown in Fig. 12(c). During transients, this voltage deviates from its reference voltage. However, it is brought back to the reference value once steady state is reached. Fig. 12(d) shows the phaserm's compensator current which is large, nearly 47 A, during the sag period. These waveforms confirm that the DSTATCOM has the capability to mitigate deep sag independent of duration. However, it requires a high current rating of the VSI.

### C. Operation During Load Change

To show the impact of load changes on system performance, load is increased to 140% of its nominal value. Under this condition, the traditional method gives less power factor as the compensator will supply more reactive current to maintain the reference voltage. The voltage and current waveforms, as shown in Fig. 13(a), confirm this. In proposed method, a load change will result in small deviation in terminal voltage from its reference voltage. Compensator just needs to supply extra reactive current to overcome this small extra feeder drop, hence, nearly UPF is maintained while regulating the terminal voltage at its reference voltage. It is evident from Fig. 13(b).

## V. CONCLUSION

In this paper, a control algorithm has been proposed for the generation of reference load voltage for a voltage-controlled DSTATCOM. The performance of the proposed scheme is compared with the traditional voltage-controlled DSTATCOM. The proposed method provides the following advantages: 1) at nominal load, the compensator injects reactive and harmonic components of load currents, resulting in UPF; 2) nearly UPF is maintained for a load change; 3) fast voltage regulation has been achieved during voltage disturbances; and 4) losses in the multi level inverter and feeder are reduced considerably, and have higher sag supporting capability with the same VSI rating compared to the traditional scheme. The simulation results show that the proposed scheme provides DSTATCOM, a capability to improve several PQ problems (related to voltage and current).

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