An Efficient Method for the Design of a Look-Up-Table (LUT) using Reversible Fault Tolerant Gates

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ABSTRACT:

This paper presents the design of a reversible fault tolerant architecture for LUT (Look-Up-Table). A new 6×6 fault tolerant reversible gate is introduced for the design of an efficient LUT. The proposed design achieves the improvement in terms of number of gates, Quantum cost and unit delay compared to the best known existing approach. The proposed LUT can be used to implement any combinational Boolean function with minimum number of transistors which satisfies the fault tolerant property.

Keywords: LUT (Look-Up-Table), Reversible logic, Fault Tolerant, Boolean Function.

1. INTRODUCTION:

Now-a-days the reduction of power dissipation is the main requirement in the field of VLSI. From the past few years, the reversible logic has received a great attention to prevent this problem of power dissipation. According to Moore's Law the transistor size is going to decrease from year to year and increase in the number of transistors per unit area. Low energy dissipation is possible with the use of Reversible logic. An operation is said to be physically reversible if there is no energy to heat conversion and no change in entropy. In reversible logic, the state of the signals prior to the operation can be predicted by its state just after the computational device i.e. any information regarding the computational logic can ever be lost. The power consumption comparison can be made using Microwind DSCH [4].

2. THE CONCEPT OF REVERSIBLE LOGIC:

Reversibility in computing implies that no information regarding the computational states can ever be lost, so the recovery of any earlier stage can be done by computing backward. This is termed as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. The process of no energy dissipation to heat is known as physical reversibility. Practically, in most of the cases the absolute and perfect physical reversibility is unachievable. In computing systems, the heat is given off when voltage levels change from negative to positive: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages as well. Eventually, these will also have to be reversible to provide optimal efficiency.

3. MOTIVATION BEHIND REVERSIBLE LOGIC:

High-performance chip releases large amount of heat energy which impose practical limitations on the performance of system. Reversible circuits that conserve information, by un-computing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. There is an improvement in energy efficiency using this Reversible computing which will fundamentally affect the speed of circuits such as micro-circuits and therefore the speed of most computing applications. Reversible computing is also required to improve the portability of any design which in turn let the circuit element sizes to reduce to atomic size limits and hence device results in more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored.

4. REVERSIBLE LOGIC GATES:

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one-to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- Number of Gates (N): The number of reversible gates used in circuit.

- Constant Inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- Garbage Outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- Quantum Cost (QC): It is referred to the cost of the circuit in terms of the primitive gate cost. It is calculated from the number of primitive reversible logic gates (1×1 or 2×2) required for the realization of the circuit.

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The below figure shows the basic reversible fault tolerant gate (Fredkin gate). It is a 3×3 reversible gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). It can be concluded from the truth table that the parity is preserved from input to output. Hence, the Fredkin gate is Fault tolerant gate.
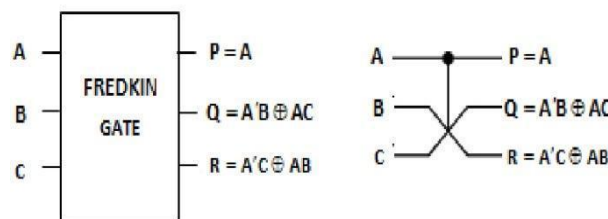
Fig.1: Fredkin gate (FRG)
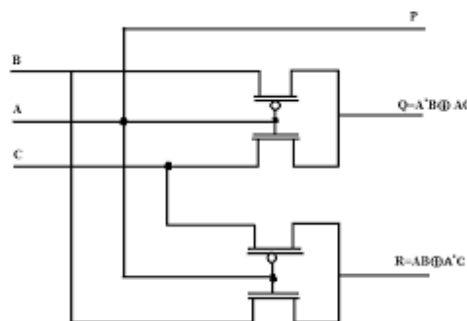
Fig.2: Transistor realization of FRG

Table.1: Truth table for FRG

Input			Output of Fredkin			Parity check
A	B	C	P	Q	R	
0	0	0	0	0	0	Even
0	0	1	0	0	1	Odd
0	1	0	0	1	0	Odd
0	1	1	0	1	1	Even
1	0	0	1	0	0	Odd
1	0	1	1	1	0	Even
1	1	0	1	0	1	Even
1	1	1	1	1	1	Odd

5. PROPOSED REVERSIBLE GATE:

MSB (Mubin-Sworna-Babu):

It is a 6×6 reversible fault tolerant gate having six inputs and six outputs [5]. The below figure represents the proposed MSB gate having input vector is [A,B,C,D,E,F] and output vector is [P,Q,R,S,T,U] with its quantum realization
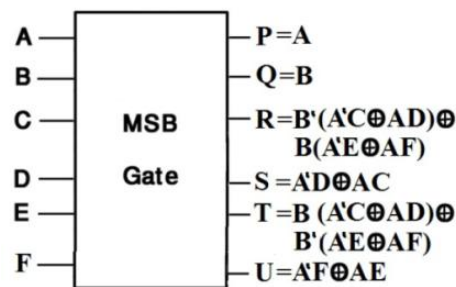
Fig.3: Block diagram of MSB gate
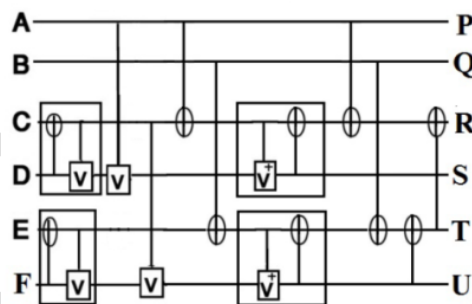
Fig.4: Quantum realization of MSB gate
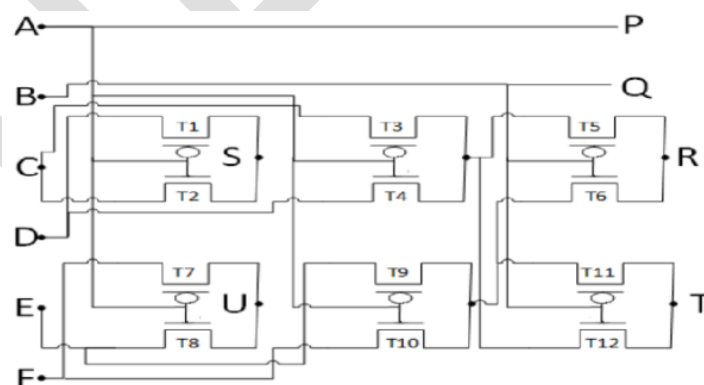
Fig.5: Transistor realization of the proposed MSB Gate

Table demonstrates the unique one-to-one correspondence and parity preservation between input (A,B,C,D,E,F) and output (P,Q,R,S,T,U) of the proposed MSB gate. For any input combination, corresponding output combination shows the same parity that is $A \oplus B \oplus C \oplus D \oplus E \oplus F = P \oplus Q \oplus R \oplus S \oplus T \oplus U$ as well as reversibility of the proposed gate.

6. PROPOSED REVERSIBLE FAULT TOLERANT N-INPUT LUT:

An 8×1 RFT multiplexer is proposed using two MSB and one FRG gates and a 16×1 RFT multiplexer using five MSB gates which are actually an 3-input and 4-input LUT as illustrated in the following figures. In this figure, 1/0 have been stored using our proposed D-Latches. Similarly we can design an n-input LUT with our proposed architecture.

(a)   (b)

Fig.6: Block diagram of proposed RFT (a) 3-input LUT (b) 4-input LUT

Table.2: Truth table of MSB gate

| Input						Output						Parity	Input						Output						Parity
A	B	C	D	E	F	P	Q	R	S	T	U		A	B	C	D	E	F	P	Q	R	S	T	U	
0	0	0	0	0	0	0	0	0	0	0	0	Even	1	0	0	0	0	0	1	0	0	0	0	0	Odd
0	0	0	0	0	1	0	0	0	0	0	1	Odd	1	0	0	0	0	1	1	0	0	0	1	0	Even
0	0	0	0	1	0	0	0	0	0	1	0	Odd	1	0	0	0	1	0	1	0	0	0	0	1	Even
0	0	0	0	1	1	0	0	0	0	1	1	Even	1	0	0	0	1	1	1	0	0	0	1	1	Odd
0	0	0	1	0	0	0	0	0	1	0	0	Odd	1	0	0	1	0	0	1	0	1	0	0	0	Even
0	0	0	1	0	1	0	0	0	1	0	1	Even	1	0	0	1	0	1	1	0	1	0	1	0	Odd
0	0	0	1	1	0	0	0	0	1	1	0	Even	1	0	0	1	1	0	1	0	1	0	0	1	Odd
0	0	0	1	1	1	0	0	0	1	1	1	Odd	1	0	0	1	1	1	1	0	1	0	1	1	Even
0	0	1	0	0	0	0	0	1	0	0	0	Odd	1	0	1	0	0	0	1	0	0	1	0	0	Even
0	0	1	0	0	1	0	0	1	0	0	1	Even	1	0	1	0	0	1	1	0	0	1	1	0	Odd
0	0	1	0	1	0	0	0	1	0	1	0	Even	1	0	1	0	1	0	1	0	0	1	0	1	Odd
0	0	1	0	1	1	0	0	1	0	1	1	Odd	1	0	1	0	1	1	1	0	0	1	1	1	Even
0	0	1	1	0	0	0	0	1	1	0	0	Even	1	0	1	1	0	0	1	0	1	1	0	0	Odd
0	0	1	1	0	1	0	0	1	1	0	1	Odd	1	0	1	1	0	1	1	0	1	1	1	0	Even
0	0	1	1	1	0	0	0	1	1	1	0	Odd	1	0	1	1	1	0	1	0	1	1	0	1	Even
0	0	1	1	1	1	0	0	1	1	1	1	Even	1	0	1	1	1	1	1	0	1	1	1	1	Odd
0	1	0	0	0	0	0	1	0	0	0	0	Odd	1	1	0	0	0	0	1	1	0	0	0	0	Even
0	1	0	0	0	1	0	1	0	0	0	1	Even	1	1	0	0	0	1	1	1	1	0	0	0	Odd
0	1	0	0	1	0	0	1	1	0	0	0	Even	1	1	0	0	1	0	1	1	0	0	0	1	Odd
0	1	0	0	1	1	0	1	1	0	0	1	Odd	1	1	0	0	1	1	1	1	1	0	0	1	Even
0	1	0	1	0	0	0	1	0	1	0	0	Even	1	1	0	1	0	0	1	1	0	0	1	0	Odd
0	1	0	1	0	1	0	1	0	1	0	1	Odd	1	1	0	1	0	1	1	1	1	0	1	0	Even

0	1	0	1	1	0	0	1	1	1	0	0	Odd		1	1	0	1	1	0	1	1	0	0	1	1	Even
0	1	0	1	1	1	0	1	1	1	0	1	Even		1	1	0	1	1	1	1	1	1	0	1	1	Odd
0	1	1	0	0	0	0	1	0	0	1	0	Even		1	1	1	0	0	0	1	1	0	1	0	0	Odd
0	1	1	0	0	1	0	1	0	0	1	1	Odd		1	1	1	0	0	1	1	1	1	1	0	0	Even
0	1	1	0	1	0	0	1	1	0	1	0	Odd		1	1	1	0	1	0	1	1	0	1	0	1	Even
0	1	1	0	1	1	0	1	1	0	1	1	Even		1	1	1	0	1	1	1	1	1	1	0	1	Odd
0	1	1	1	0	0	0	1	0	1	1	0	Odd		1	1	1	1	0	0	1	1	0	1	1	0	Even
0	1	1	1	0	1	0	1	0	1	1	1	Even		1	1	1	1	0	1	1	1	1	1	1	0	Odd
0	1	1	1	1	0	0	1	1	1	1	0	Even		1	1	1	1	1	0	1	1	0	1	1	1	Odd
0	1	1	1	1	1	0	1	1	1	1	1	Odd		1	1	1	1	1	1	1	1	1	1	1	1	Even

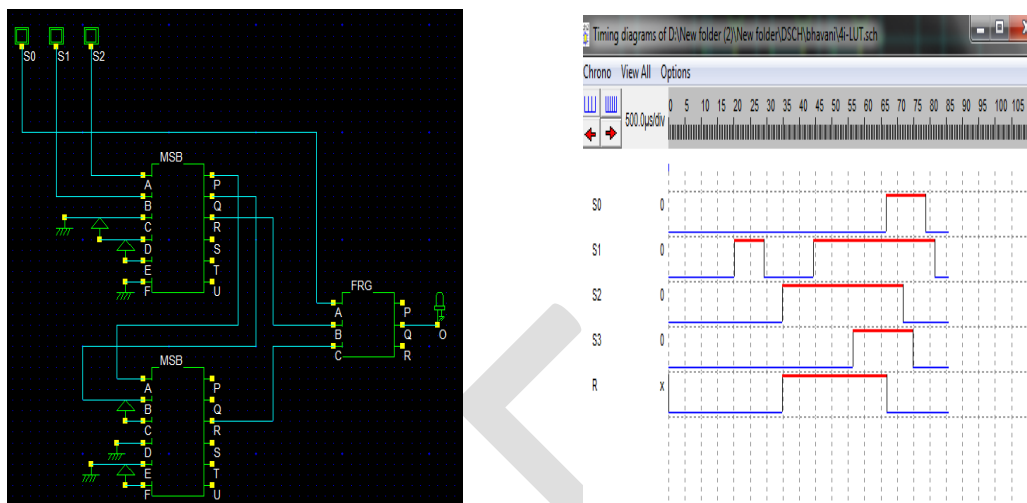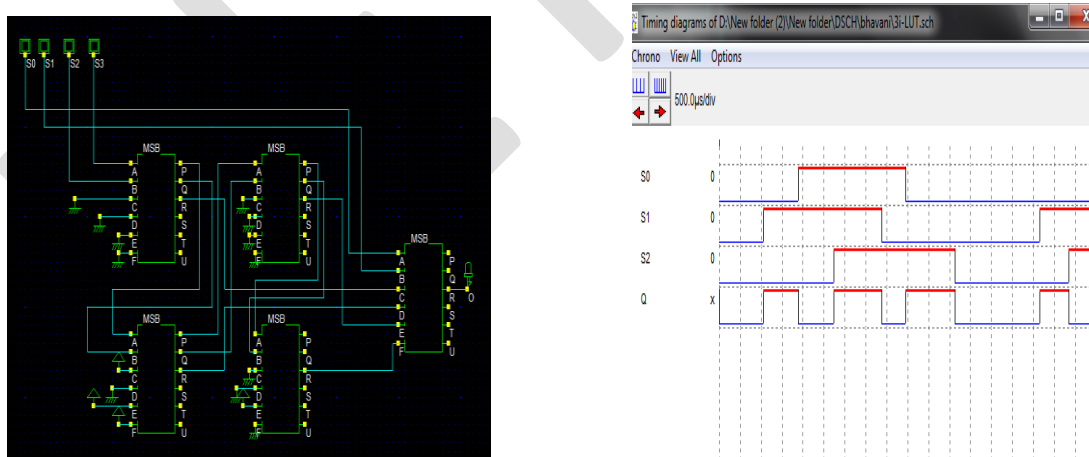## 7. SIMULATION RESULTS:

1) FRG GATE:
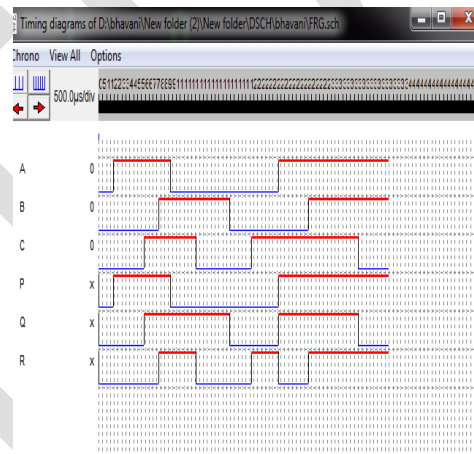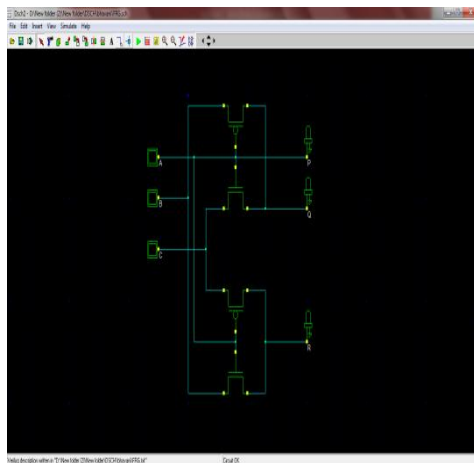
2) MSB GATE:
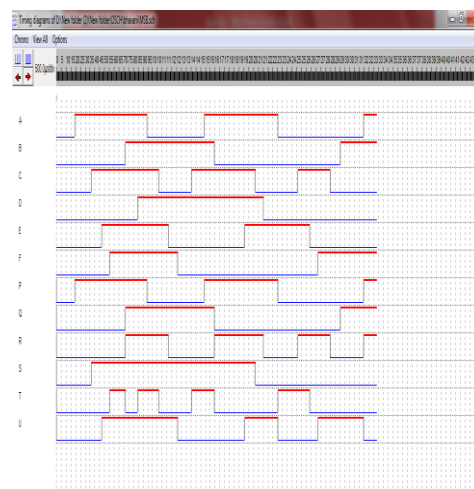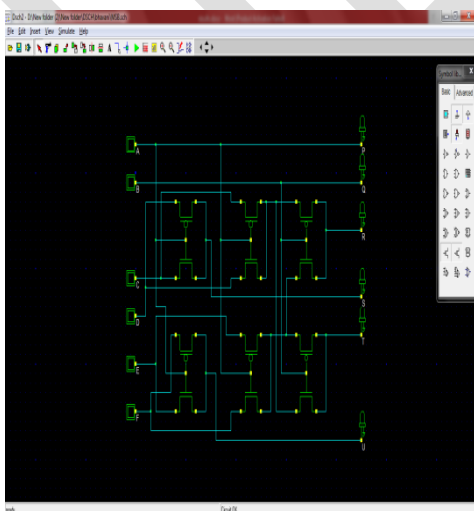
Applications for the Proposed LUT:

The look-up-tables are simply known to store the truth table of a circuit. The design of these reversible LUT is used for the implementation of any combinational logic.

(a) Full adder using 3-input:

(b) Implementing a Boolean logic using 4-input LUT:

Comparative Analysis of LUT:

The following table (Table.3) shows the comparison of the design of Look-Up-Table using the previous existing methods and also with the proposed reversible fault tolerant gate. The comparison is made between the terms: Number of gates required, Transistor count, Garbage outputs, Quantum cost and Unit delay for the entire design. It confirms that the number of transistors required for LUT design is low compared to the previous reversible logic designs.

Table.3: Comparison among the various reversible design methodologies.

LUT Size	3-Input LUT				
	Number of gates	Transistors	Garbage	Quantum cost	Unit delay
Design of a compact reversible fault tolerant field programmable gate array [3]	7	70	35	10	7
Design of a reversible logic block of field programmable gate array [4]	19	166	119	24	19
Design of a LUT-based reversible field programmable gate array [5]	15	150	119	24	15
Using FRG and MSB gate (Proposed)	3	28	29	10	3
LUT Size	**4-Input LUT**				
Design of a compact reversible fault tolerant field programmable gate array [3]	15	150	75	19	15
Design of a reversible logic block of field programmable gate array [4]	39	342	243	50	39
Design of a LUT-based reversible field programmable gate array [5]	31	310	243	50	31
Using MSB gate (Proposed)	5	60	60	19	5

8. CONCLUSION:

Hence the designs of reversible fault tolerant LUT (Look-Up-Table) using a new reversible fault tolerant gate namely MSB (Mubin-Sworna-Babu) gate is done with efficient results. The Transistor count and unit delay are considerably low for the proposed system compared to the existing methodologies. Finally using both 3-input and 4-input LUT's to design a full adder and a Boolean function respectively. The proposed reversible gate avails to design an efficient LUT. These LUT's can be applied for the design of Xilinx-based FPGA designs.

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