# IMPLEMENTATION OF MULTIPLIER USING ADVANCED CARRY SELECT ADDER

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## ABSTRACT

Multipliers are major components of any processor or computing machine. Digital signal processors (DSP) and performance of microcontrollers are evaluated on the basis of number of multiplications performed at unit time. Hence multiplier architectures are bound to increase the efficiency of the system. With the additional highlights, implementing multiplier using reversible logic further reduces power dissipation as it is another important constraint in a VLSI design, which cannot be neglected. With DSP applications evolving continuously, there is continuous need for improved multipliers which are faster and power efficient. Reversible logic is a new and promising field which addresses the problem of power dissipation. It has been shown to consume zero power theoretically. Therefore, in this paper we implement multiplier algorithm using reversible logic thereby addressing two important issues – speed and power consumption of implementation of multipliers. In this work, 16x16multiplier is designed by using reversible logic gates and advanced carry select adder there by reducing the complexity of multiplier. The advanced carry select adder consists of ripple carry adder(RCA) and a Binary to Excess-1 converter(BEC). This multiplier can find its application in various fields like convolution, filter applications, cryptography, and communication.

**Key words:** Multiplier, Advanced carry select adder, reversible logic gates, power, area, delay, RCA, BEC.

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## INTRODUCTION

In current digital systems, power consumption, area and delay have become the most important factors to be considered while designing a system. Multiplication and addition are the important fundamental functions of any system and is used in many DSP applications like digital filtering, digital communications, spectral analysis. Many current devices with DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay and power of a multiplier is an essential part of satisfying the overall design.

Addition is the heart of multiplication and many other arithmetic operations. It is observed that in microprocessors and RISC processors, addition is performed on88.4% of total instructions involving the ALU and high active register banks contribute to 71% of total power dissipation [1]. Generally conventional multipliers use carry select adder for addition purpose.

The Carry Select Adder[6] is used in many computational systems to resolve the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA)[7] to generate partial sum and carry by considering carry input Cin = 0 and Cin = 1, then the final sum and carry are selected by the multiplexers (mux)[7].

The proposed system increases speed by using advance carry select adder[8], also reduces the power dissipation by using reverse logic gates[2] in generating partial products .Multiplication involves generation of partial products and addition of partial products, for which we used peres reverse logic gate[3] for generation of partial products and advanced carry select adder[8] is used to add the partial products. Instead of using pair of RCA's in regular CSLA, here we are using one RCA with cin=0 and Binary to Excess-1 Converter (BEC) instead of second RCA with Cin = 1 to achieve lower power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Ripple Carry Adder (RCA)[7].

## PROPOSED SYSTEM

The primary focus of this work is realization of low power and high speed operation of the conventional CSLA(carry select adder) circuit through reverse logic operation. Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. A Reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. In thisperes reversible logicgate is used in generation of partial products[2].

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## BLOCK DIAGRAM OF MULTIPLIER

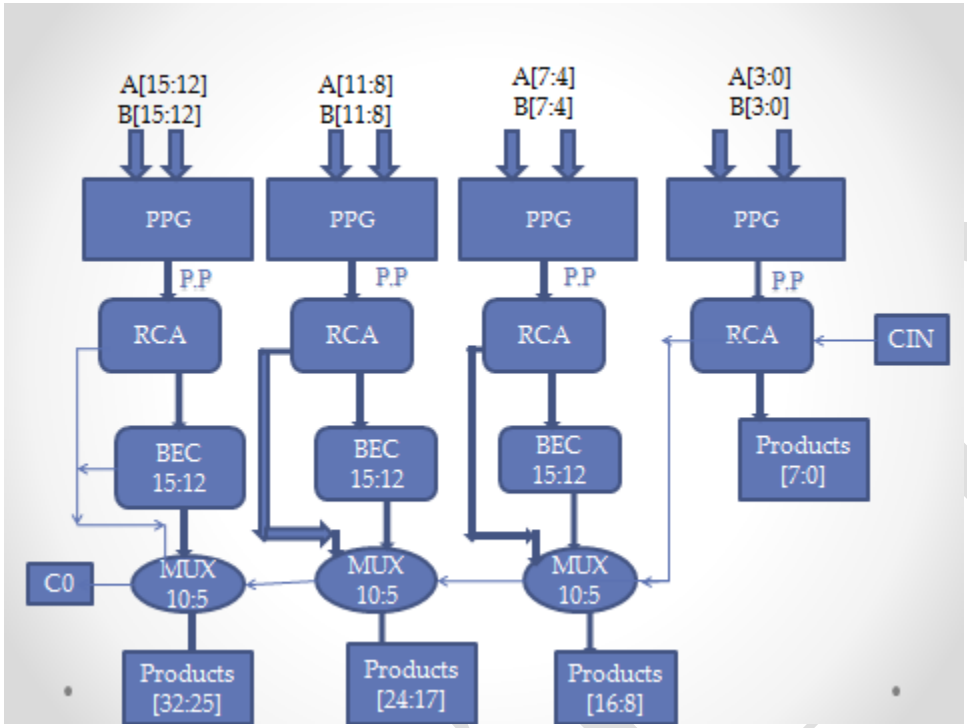


**Fig 1: Multiplier Block**

## PERES GATE:

Peres Gate (PG) is composed of two XOR gate shown in Figure 2 and one AND gate[2]. The input vector is I (A, B, C) and the output vector is O (P, Q and R). The output is defined by P = A, Q = A⊕B and R=AB⊕C[5].

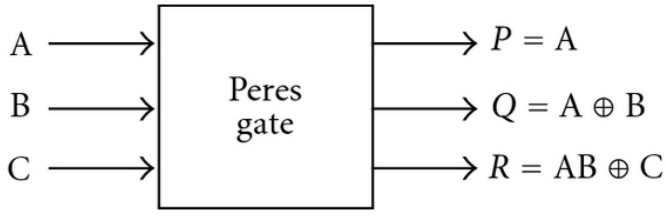


**Fig 2: Peres Gate**

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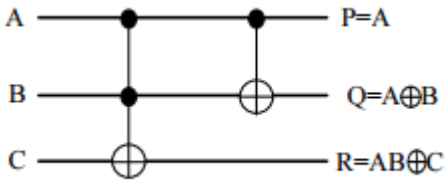
**Table 1. Truth table of peres gate**

| INPUT | | | OUTPUT | | |
|---|---|---|---|---|---|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |




In this A, B and C are inputs, Where A and B may be 0 or 1. Since we are performing multiplication of two operands C is taken as 0 depending on the output R. Each peres gate multiplies two single bit inputs. In this paper we are performing 16 bit multiplication and so we use 16 peres gates for generation of 16 partial products. [4]

## REVERSIBLE MULTIPLIER

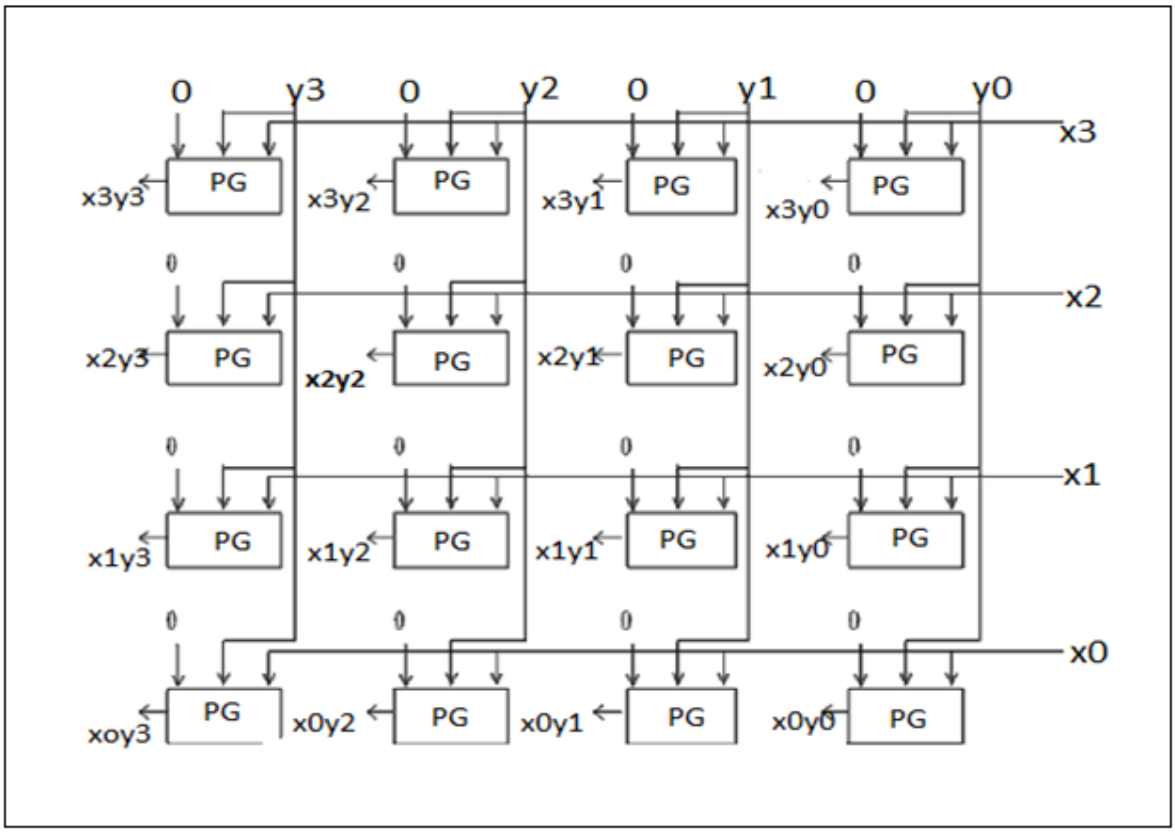



**Fig 3: Partial Product Generator(PPG)**

## ADVANCED CARRY SELECT ADDER(ACSA)

In digital adders, the speed of addition is limited due to the time taken by the carry signal to propagate through the adder. The regular carry select adder (R-CSLA)[6] was introduced to mitigate the problem of carry propagation delay by independently generating multiple carries and then selecting the correct sum and carry outputs depending on the value of previous carry [4]. As previously discussed, this type of CSLA (i.e., R-CSLA) was not area efficient due to the use of pair of RCAs (each forCin=0andCin=1 ) to produce the final sum and carry output[7].

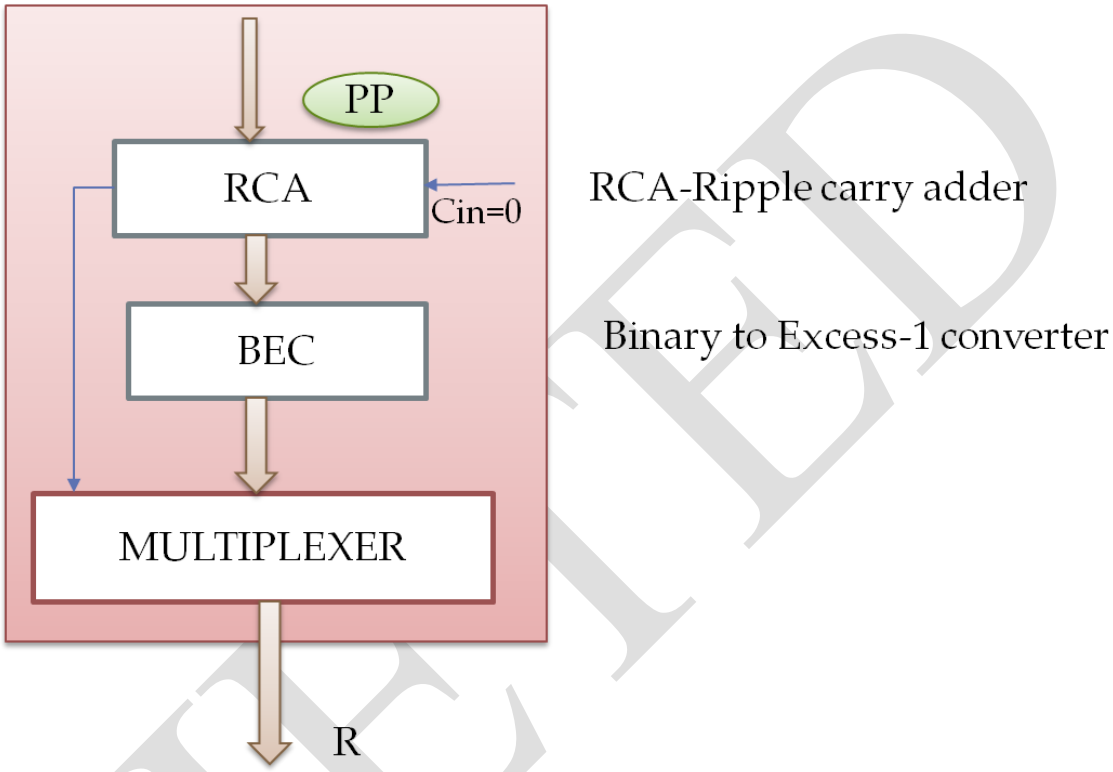



**Fig 4: Modified CSA**

The modification to the conventional CSLA structure has been presented in reference [8]. It realizes reduction of area and power consumption through the use of a binary-to-excess code 1 (BEC-1) converter as depicted in Figure. The n-bit RCA with Cin=1 is replaced with (n+1) bit BEC-1 logic in the conventional CSLA adder.

## RIPPLE CARRY ADDER(RCA)

RCA(ripple carry adder ) performs the addition of generated partial products. At each stage in the ACSLA(advanced carry select adder) we used 4 bit RCA(ripple carry adder) with carry in(cin) as 0, which adds two 4-bit binary numbers and generates sum and carry. Since we require 16 bit addition we used four RCA's(ripple carry adders)[7].

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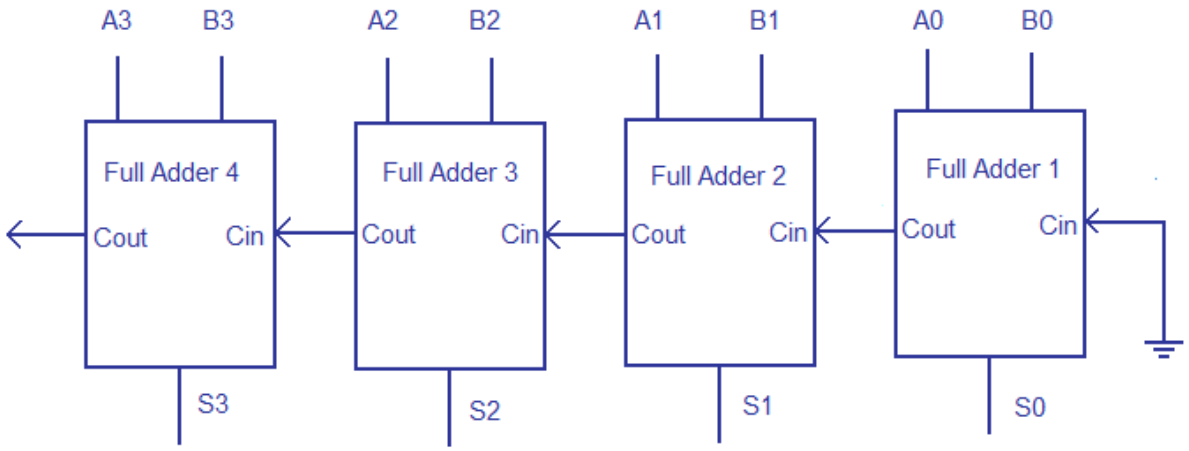


**Fig 5: Ripple carry adder**

## BINARY TO EXCESS-1 CONVERTER(BEC)

The basic use of binary to excess-1 converter(BEC) instead of RCA with Cin=1 in the regular CSA(carry select adder) to achieve lower area and power consumption. It uses lesser number of logic gates compared to conventional CSA. It takes input from RCA and converts into excess-1 so that it becomes the sum with carry in as 1[9].

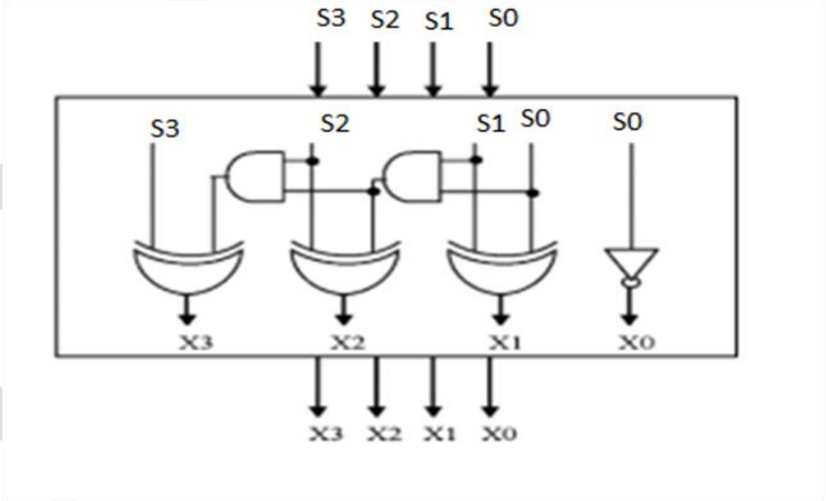


**Fig 6: Binary to Excess-1 converter**

Since we know the carry in at first stage is 0(zero) ,there is no need of BEC in the first stage. The boolean expression of 4-bit BEC is listed as

X0=~S0
X1=S0^(S0&S1)
X2=S2^(S0&S1)
X3=S3^(S0&S1&S2)

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## MULTIPLEXER

It is generally used to select one output among many inputs using select lines. In proposed model multiplexer take two inputs i.e with carry in 0 and BEC output and selects one among them depending on the previous stage carry. Here the carry out of the previous stage acts as select lines for multiplexer. If the carry of the previous stage is 0(zero), then it selects RCA output and if the carry in of the previous stage is 1, multiplexer selects BEC output.

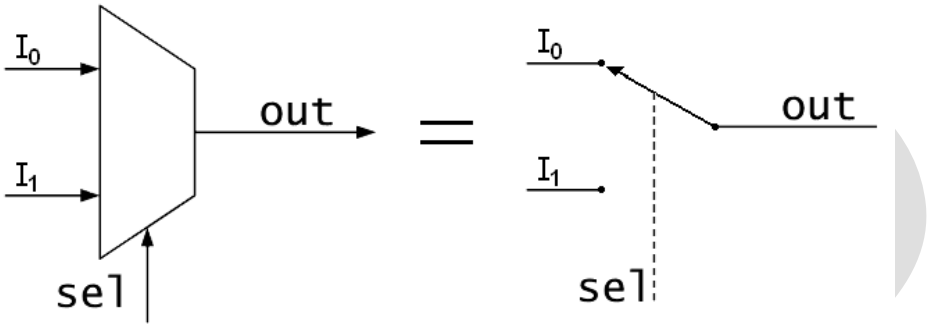


**Fig 7: -2-Input Mux**

## IMPLEMENTATION

The 16×16 multiplication operation is designed using Verilog HDL and simulation is performed in Modelsim and xilinx.

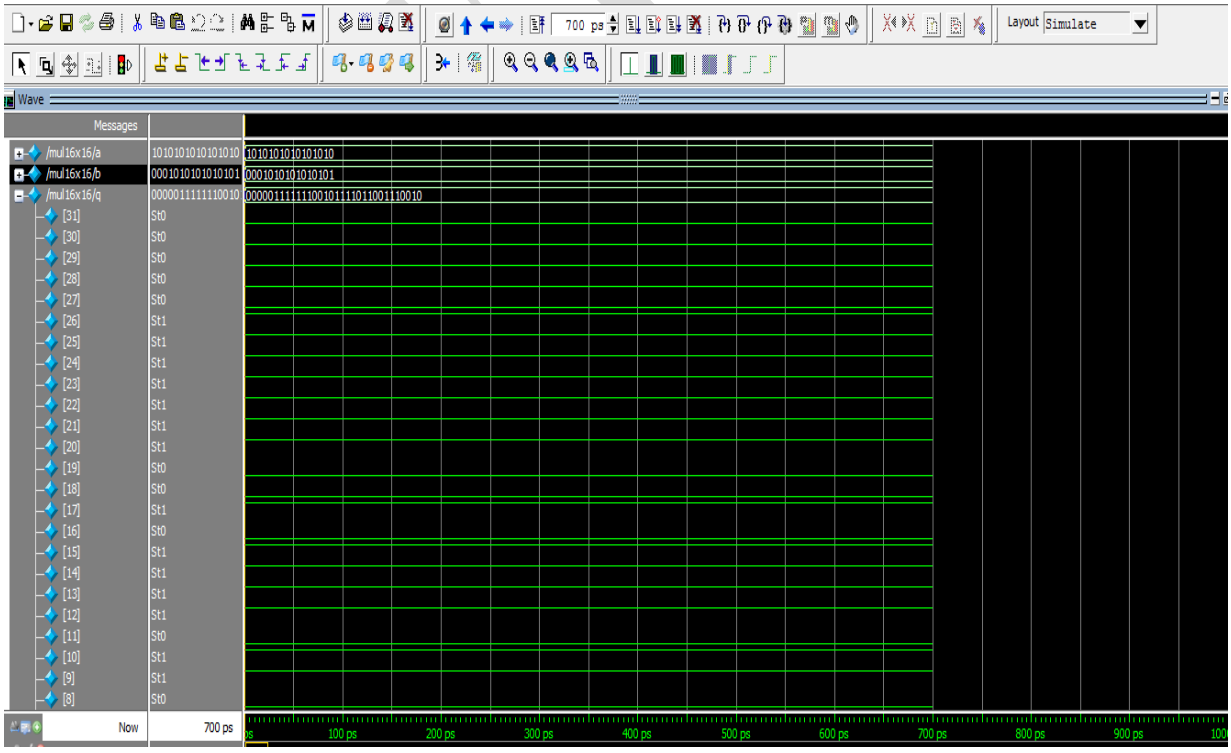


**Fig 7: Output of multiplier**

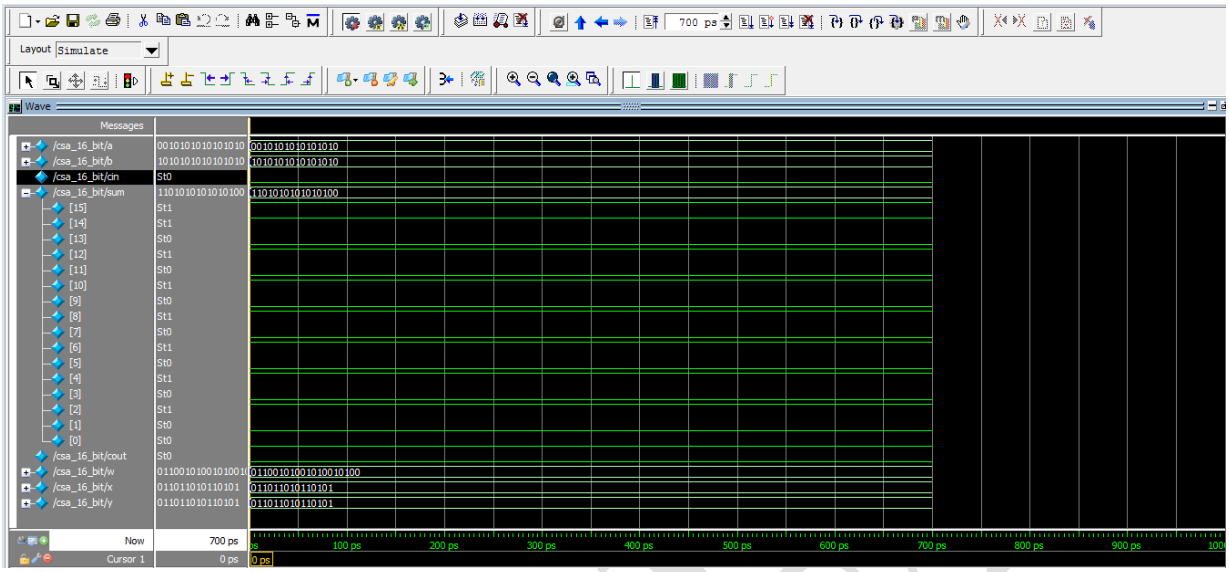


**Fig 8: output of ACSA**

**Table 2. Comparision Of Different Adders[12]**

| Parameter | RCA | CLA | CSA | ACSA |
|---|---|---|---|---|
| **Delay(ns)** | 24.686 | 24.686 | 26.9 | 16.29 |
| **Power(W)** | 1.7318 | 1.9668 | 0.112 | 0.009 |

**Table 3. Comparision Of Different Multiplier[11]**

| Parameter | Array | Wallace tree | Booth | Proposed |
|---|---|---|---|---|
| Delay(ns) | 91.456 | 63.873 | 232 | 41.14 |
| Power(W) | 0.086 | 0.054 | 0.067 | 0.015 |

## CONCLUSION

In this paper, we presented a multiplier circuit using reversible logic gates (Peres gates) for generation of partial products and advanced carry select adder to add the generated partial products. The proposed multiplier circuit is better than the existing designs in terms of number of logic gates, and constant inputs. With an overhead of increased area, the proposed multiplier has a low power dissipation and delay time thereby increasing the efficiency of the system.

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