# Design and Implementation of High Speed and Area Efficient Digit Serial FIR Filter

**P.Prashanti**[#1]
#1 Dept. of ECE BVRITH

## ABSTRACT

Many applications in DSP, telecommunications, graphics, and control have computations that either involve a large number of multiplications of one variable with several constants, or can easily be transformed to that form. A proper optimization of this part of the computation, which we call the multiple constant multiplication (MCM) problems, often results in a significant improvement in several key design metrics, such as throughput, area, and power. In the last few years, algorithms and architectures have been introduced to design bit-parallel MCM which has higher complexity and less importance is given to digit- serial MCM design. Bit-parallel architectures may be faster than necessary and occupy considerable amount of area. On the other hand, digit-serial architectures decrease complexity, occupy less area and low power operations at the cost of an increased delay. In digit-serial design we basically implement Distributive Arithmetic and the common sub-expression elimination. In this paper, we are going to develop optimized algorithms to address this problem and achieve better performance and high efficiency.

**Key words:** Common sub-expression elimination, digit serial arithmetic, finite impulse response (FIR) filters, graph based algorithm, multiple constant multiplication (MCM).

**Corresponding Author: P.Prashanti, Asst Prof, Dept of ECE, BVRITH**

## INTRODUCTION

In electronic applications, adders are most widely used. Applications where these adders are used are multipliers, Digital Signal Processing (DSP) to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes, adders come in to the picture. As we know that in microprocessors, millions of instructions are performed per second, so speed of operation is the most important factor to be considered while designing multipliers. Due to device portability, fabrication of device should be small and power consumption should be low. Devices like Mobile, Laptops etc. require more battery backup. Digital filters are generally classified into two types, Finite Impulse Response filters and Infinite Impulse Response filters [1]. Here FIR filter is going to be designed and the analysis of word length is made. An FIR filter is defined as a filter that has impulse response for a finite duration of time. Direct form and transposed form are the two basic FIR structures as illustrated in Fig 1 and 2. Although transposed form is generally preferred because of its high performance and power efficiency, in the direct form, the multiple constant multiplication (MCM)/accumulation (MCMA) module performs the concurrent multiplications of individual delayed signals and respective filter coefficients, followed by the accumulation of all the products. Thus, the operands of the

multipliers in MCMA are delayed input signals x [n−i] and coefficients. In transposed form, where in the multiplication of filter coefficients with the filter input is realized, there is significant impact on the complexity and performance of the design because a large number of constant multiplications are required. This is generally known as the multiple constant multiplications (MCM) operation.

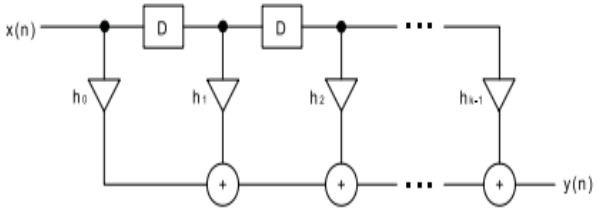


**Fig 1: Direct form**

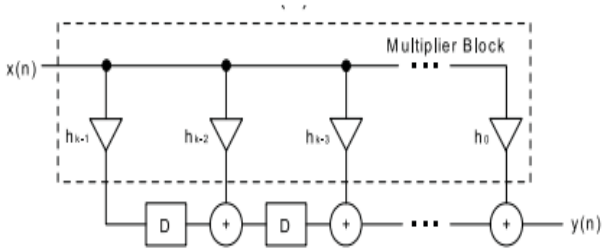


**Fig 2: Transposed form**

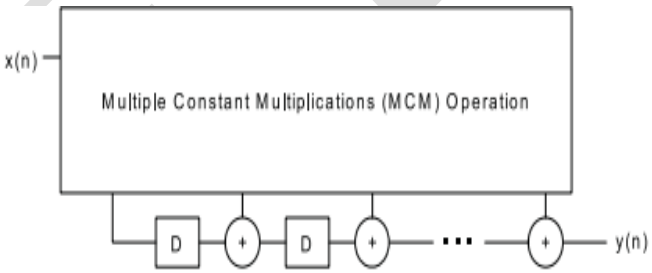


**Fig 3: Transposed form with an MCM block**

Multiplication of filter coefficients with the input data is generally implemented under a shift adds architecture, where each constant multiplication is realized using addition/subtraction and direct form with an MCM block as shown in Fig 3.

## EXISTING SYSTEM

Multiple constant multiplication (MCM) constitutes a typical fixed-point arithmetic operation in digital signal Processing. It focuses on a lot of research on high-speed and low power devices in communication systems and signal processing systems. In multiplier less MCM, multipliers are replaced by simpler components such as adders and hard-wired shifts (adders in

our paper include also subtractions as their hardware costs are similar). By using the negative digits in signed-digit representations, coefficients may be synthesized with few adders, therefore area and delay of circuit can be reduced. Initially an FIR filter is implemented by using bit-parallel multiple constant multiplications. This operation dominates the complexity of many digital signal processing systems. Also bit parallel design requires excessive hardware.

## PROPOSED SYSTEM

In this paper, we implement digit-serial FIR filter. When the bit-parallel implementation cannot meet the delay requirements, digit-serial computation is used [6]. Thus, the trade-off between area and delay can be explored by changing the digit-size. Here, the data words are divided in to digit sets, consisting of n bits which are processed one by one. Comparing to bit-parallel design, digit-serial architectures offers lower complexity. This is possible because of the less area of digit-serial operators and is independent of data word length. The shifts require the use D flip- flops. Hence, while choosing the algorithms, the high level algorithms should be taken into account for the sharing of shift operations as well as the sharing of addition/subtraction operations in digit-serial MCM design. In this paper, we initially determine the gate-level implementation of digit serial addition, subtraction, left shift operations used in the shift-add design of digit serial MCM operations and digit serial arithmetic. Then, we introduce the exact CSE algorithm and GB algorithm that formalizes the gate-level area optimization problem [2].

## MODULES

The different modules used are Addition operation, Subtraction operation, Left shift by one time, Left shift by two times and Digit-Serial Arithmetic.

**Addition operation**: The Addition operation is performed Full Adders and Shifter.

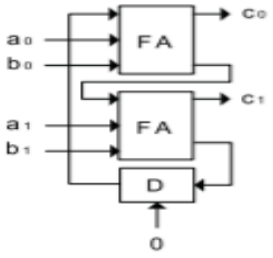


**Fig 4: Addition Operation**

**Subtraction operation:** The Subtraction operation is performed by Full Adders, Inverters and Shifter.

Issue 7, Vol. 3 (May 2017)
ISSN 2249-6149

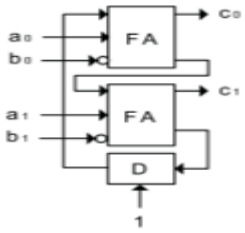


**Fig 5: Subtraction Operation**

**Left shift by one time:** In these operations the digits are moved, or shifted, to left or right. Left Shift by one time means, add a zero bit in LSB position.

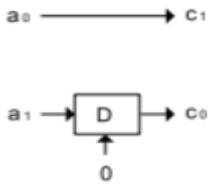


**Fig 6: Left Shift by one time**

**Left shift by two times:** Left Shift by two times means, add two bit zeros in LSB position.

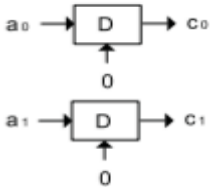


**Fig 6: Left Shift by two times**

**Digit-Serial Arithmetic:** In digit-serial designs, the input data is divided into n bits and processed serially by applying each n-bit data in parallel [4].

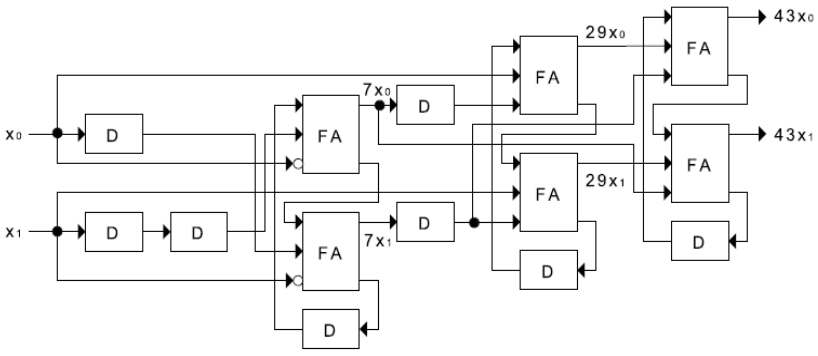


**Fig 7: Digit Serial Arithmetic**

## COMMON SUB EXPRESSION ELIMINATION (CSE) ALGORITHM

The main idea of CSE technique is to find the terms which are common between different constants and decreasing the number of repeated operations. Multipliers usually have large area and power and multiplication is expensive in hardware. In MCM the values of the constants are known beforehand. Hence, multiplication can be implemented by sequence of additions and shifts.

The idea of CSE can be demonstrated on an FIR filter design. The optimization procedure will target the minimization of the multiplier block area. The goal of CSE is to identify the bit patterns that are present in the coefficient set more than once [7]. Since it is sufficient to implement the calculation of the multiple identical expressions only once, the resources necessary for these operations can be shared.

As a simple example, consider the constant multiplications 29x and 43x. Their decompositions in binary are listed as follows: 29x = (11101) x = x << 4 + x << 3 + x << 2 + x, 43x = (101011) x = x << 5 + x << 3 + x < which requires six addition operations as illustrated. The exact CSE algorithm gives a solution with four operations by finding the most common partial products 3x = (11)x and 5x = (101)x when constants are defined under binary as illustrated in Fig 8.

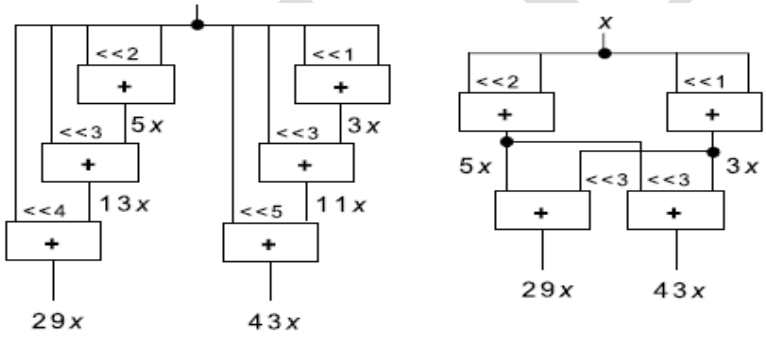


**Fig 8: CSE(Common subexpression elimination)**

## GRAPH BASE (GB) ALGORITHM

The optimization of gate-level area problem in digit-serial MCM design using CSE algorithm will decrease the area occupied and delay when compared to other techniques, When we compare CSE algorithm with GB, it gives good results. Hence, the GB algorithms, which give a good solution using less computational resources, are absolutely necessary. We find the least number of intermediate constants such that all the target and intermediate constants are synthesized using a single operation. But, while selecting an intermediate constant for the implementation of the not yet synthesized target constants for each iteration, we favor the one among the possible intermediate constants that can be synthesized using the least hardware and this will enable us to implement the target constants that are not yet synthesized in a smaller area with the available constants. After that the realization of the MCM operation happens by finding the set of target and intermediate constants, each constant is synthesized and that which yields the minimum area in the digit-serial MCM design. The area of the digit-serial MCM operation is determined as the total gate-level implementation cost of each digit-serial addition,

Issue 7, Vol. 3 (May 2017)
ISSN 2249-6149

subtraction, and shift operation. The right shift is assumed to be zero. GB algorithm finds a solution with the minimum number of operations by sharing the common partial product 7x in both multiplications as shown in Fig 9. Note that the partial product 7x = (111) x cannot be extracted from the binary representation of 43x in the exact CSE algorithm.

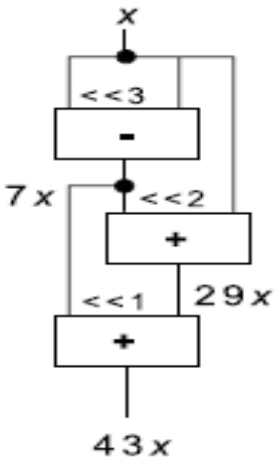


**Fig 9: Exact GB(graph based) algorithm**

## SIMULATION RESULTS

The simulation and synthesis is performed using Xilinx ISE 14.6 and the results are given below.

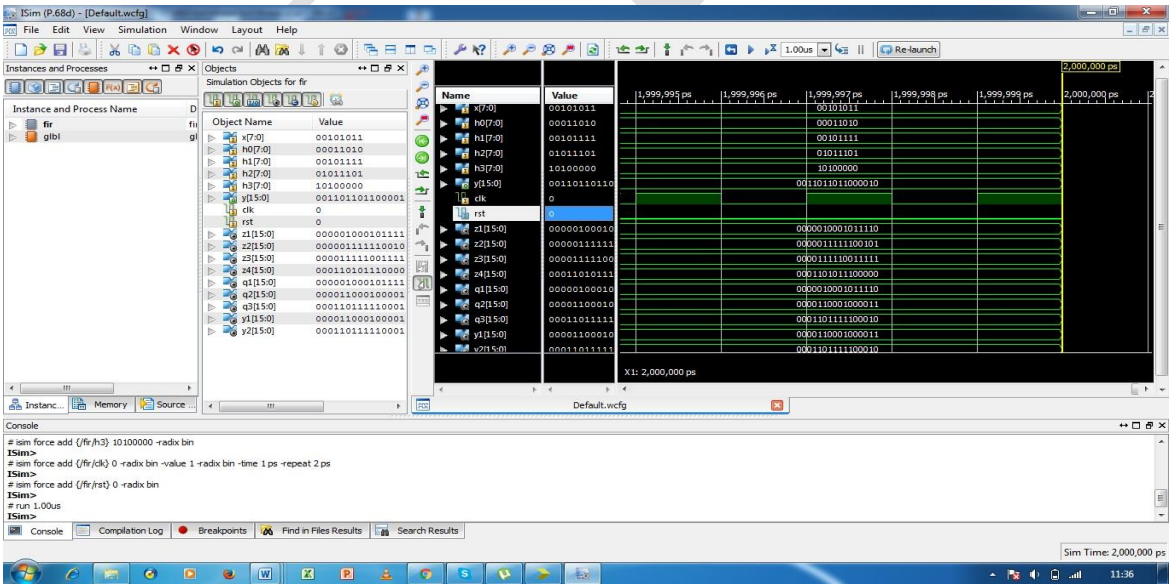

**Fig 10: Simulation Output for normal FIR filter**

Issue 7, Vol. 3 (May 2017)
ISSN 2249-6149

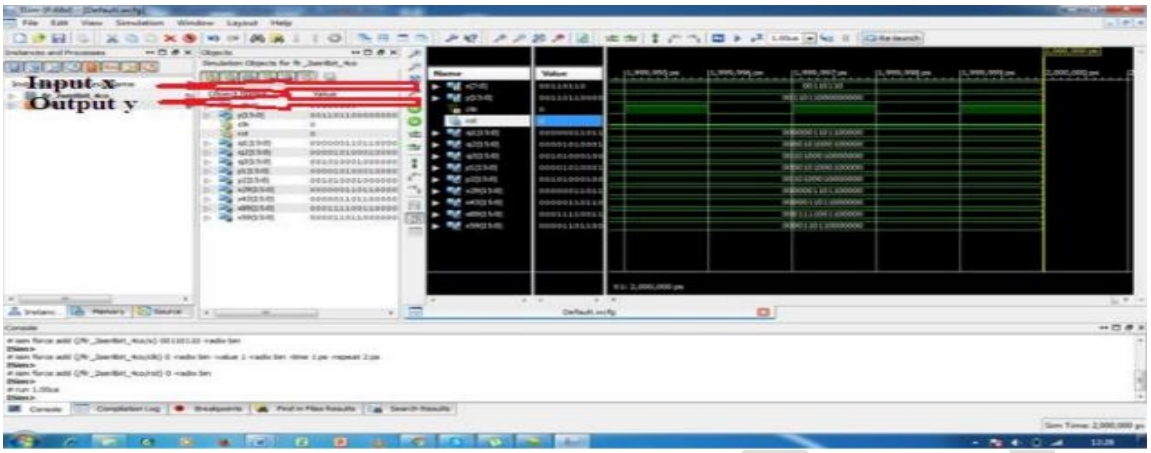


**Fig 11: Simulation Output of 4 bit FIR filter using CSE algorithm.**

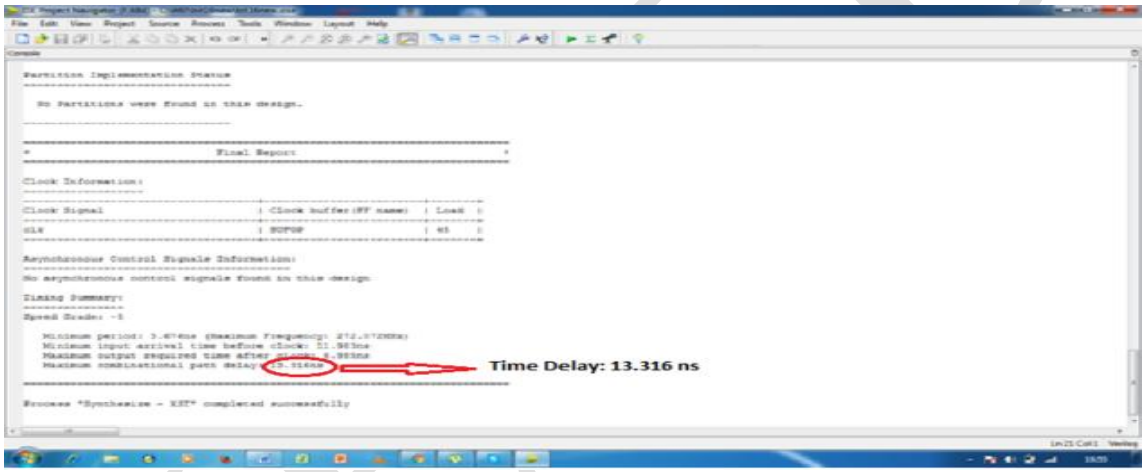


**Fig 12. Synthesis Report of Time Delay for 4 bit FIR filter using CSE algorithm**

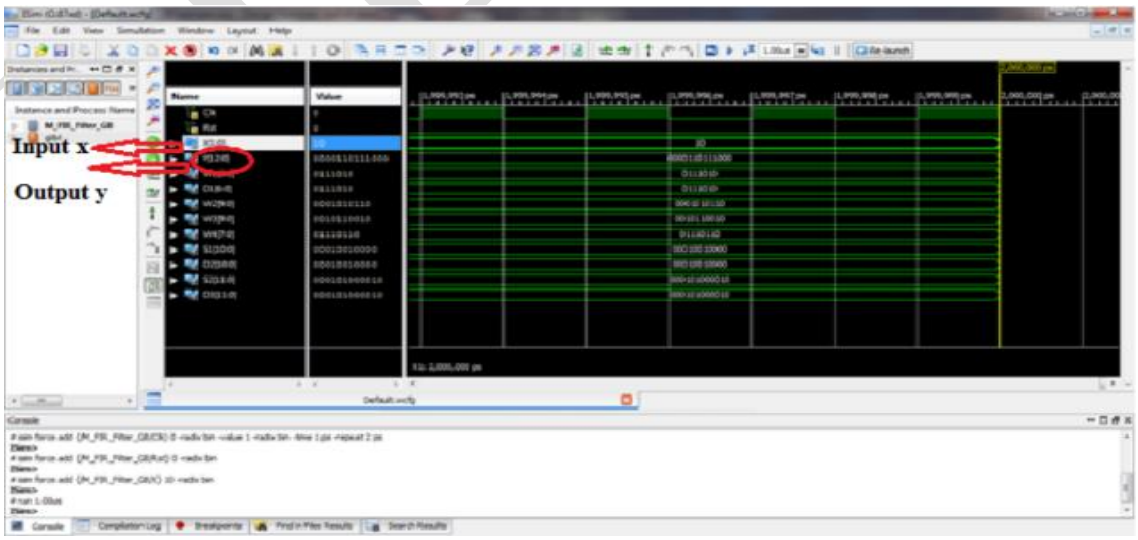


**Fig 13: Simulation output for FIR filter using GB (Graph based) algorithm**

Issue 7, Vol. 3 (May 2017)
ISSN 2249-6149

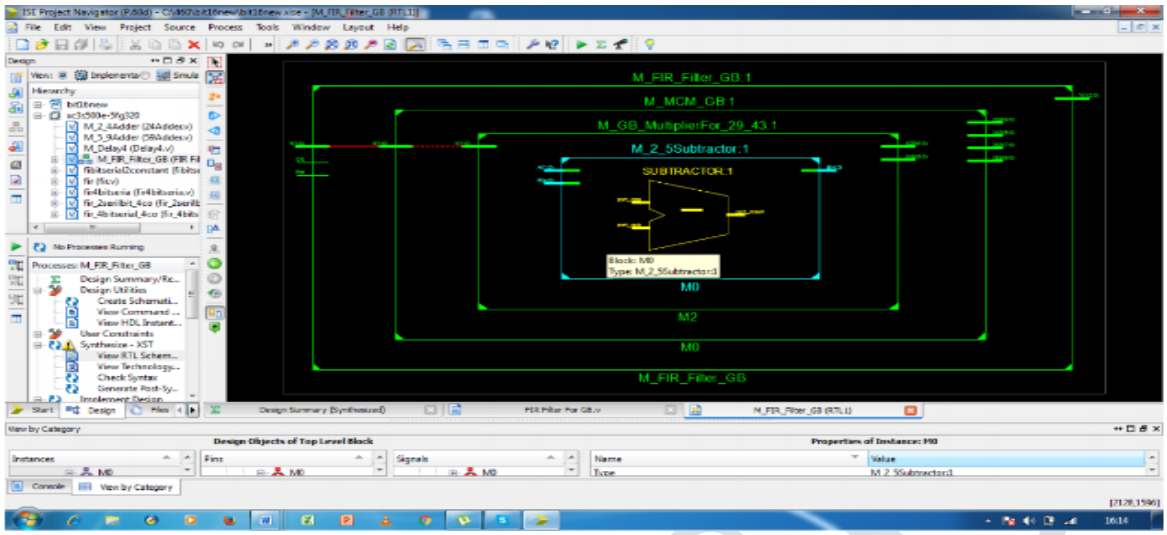


**Fig 14: RTL Schematic for FIR filter using GB algorithm**

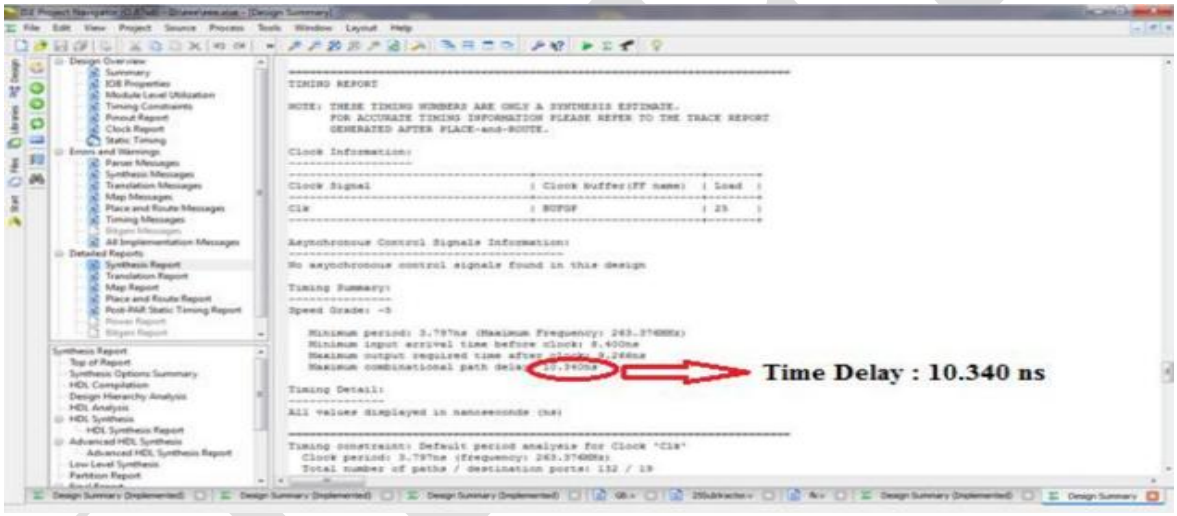


**Fig 14: Synthesis output- Time Delay for GB algorithm**

**Table1. Comparison Table**

| Digit Type | Area (LUT's) | Delay (ns) |
|---|---|---|
| FIR normal | 480 | 21.65 |
| 2 bit normal | 314 | 14.97 |
| 4 bit normal | 331 | 15.998 |
| 2 bit CSE(shift and add) | 84 | 12.613 |
| 4 bit CSE(shift and add) | 116 | 13.316 |
| GB | 5 | 6.21 |

## CONCLUSION

The digit serial FIR filter is implemented with optimal area at the gate level by considering the implementation costs of digit-serial addition, subtraction, and shift operations and with low complexity MCM architectures for digit sizes n = 2, 4. Device utilization like area and delay values are found and compared with normal FIR filter, CSE algorithm, GB algorithm. GB algorithm finds the best way to filter the given input with high speed and also occupies less area. FIR filters under the shift-adds architecture give significant area reduction and it is observed that a designer can find the circuit that fits best in an application by changing the digit size. By using digit serial architecture we can easily reduce the delay, area, cost and complexity.

## REFERENCE

[1] P. Ramesh Babu, Digital Signal Processing, sixth edition, SCITECH Publications, Jan2015.

[2] Levent Aksoy, Cristiano Lazzari, Eduardo Costa, Paulo Flores and José Monteiro, "Design of Digit-Serial FIR Filters: Algorithms,Architectures, and a CAD Tool",IEEE journal, 2013.

[3] Narendra Singh Pal, Harjit Pal Singh, R.K.Sarin and Sarabjeet Singh" Implementation of High Speed FIR Filter using Serial and Parallel Distributed Arithmetic Algorithm" International Journal of Computer Applications,2011.

[4] Shahnam Mirzaei, Anup Hosangadi, Ryan Kastner University Of California, Santa Barbara, CA 93106" FPGA Implementation of High Speed FIR Filters Using Add and Shift Method"IEEE Journal 2006.

[5] Sayyad Sarfaraz , MD. Manan Mujahid, P. Suresh" Memory based Realization of FIR filter using Advanced Look-Up Table approach " International Journal of Innovative Research in Computer and Communication Engineering,2006.

[6] Samidha Shirish Pusegaonkar , Vipin S Bhure , Amol Y Deshmukh "VLSI Architecture for Optimized Low Power Digit Serial FIR Filter using MCM" International Journal of Engineering Research and Development,2014.

[7] L.Aksoy, E. Gunes, and P. Flores, "Search algorithms for the multiple constant multiplications problem: Exact and approximate," J. Microprocess. Microsyst., vol. 34, no. 5, pp. 151–162, Aug. 2010.