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Automatic Detection and Testing Based RF Wireless Transceiver SoCs Using BISC

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ABSTRACT

A new approach to adding built-in self test (BIST) capabilities to integrated sigma-delta modulation RF transmitters is presented. An area efficient, all-digital building block generates multi-tone FM stimulus signals without compromising the performance of the RF transmitter itself. The RF signal is demodulated and digitized in a on-chip digital FM discriminator. Both blocks are fully testable using standard scan chain methods and consume a chip area of only 0.03 mm^2 in a 130 nm CMOS technology. The spectral quality and reproducibility of the test signals are suitable for inter-modulation distortion tests or PLL frequency response measurements A digital on-chip spectral analysis of the demodulated bit stream helps to allow a complete BIST, reducing even further the requirements for costly RF production test equipment. Built-In Self Calibration (BISC) strategies can also be implemented with this setup to increase the yield and to make the circuit more robust against environmental variations. When a full BIST implementation is preferable, the multiphase architecture can also be combined with a dynamic reseeding scheme that uses combinational logic instead of a ROM in order to perform the reseedings. This way the implementation area of the BIST circuitry is further reduced. Experimental results demonstrate the advantages of the proposed LFSR reseeding approach over the already known reseeding techniques.

Key words: BISC, LFSR reseeding, **LNA, ACN**, GSM transceiver, ATALANTA ATPG tool.

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INTRODUCTION

The designers of contemporary systems-on-a-chip (SoCs), in order to reduce the time-to-market and the complexity of their task, make use of various embedded cores, such as memory and processor cores. All these cores are interconnected together with some user-defined logic. However, the continuously increasing density and complexity of such systems make their testing a more and more challenging task. One of the major problems of testing complex SoCs is that of high test-data volume. The test-data storage requirements on the tester are growing rapidly as the size of the circuit under test (CUT) increases. As a result, test-data compression has become an integral part of a circuit's testing flow, as discussed in. Many works that try to tackle the high test-data volume problem have been recently presented in the open literature.

BUILT IN SELF TEST (BIST)

A built-in self-test (BIST) architecture having distributed algorithm interpretation is described. The architecture includes three tiers of abstraction: a centralized BIST controller, a set of sequencers, and a set of memory interfaces. The BIST controller stores a set of commands that generically define an algorithm for testing memory modules without regard to the physical characteristics or timing requirements of the memory modules. without regard to the physical characteristics or timing requirements of the memory modules. The sequencers interpret the commands in accordance with a command protocol and generate sequences of memory operations. The memory interfaces apply the memory operations to the memory module in accordance with physical characteristics of the memory module, e.g., by translating address and data signals based on the row-column arrangement of the memory modules to achieve bit patterns described by the commands. The command protocol allows powerful algorithms to be described in an extremely concise manner that may be applied to memory modules having diverse characteristics.

In our project, we used reseeding algorithm, which is practical and effective solution to the problem of high-test data volume. Usually, in a reseeding BIST scenario, a mixed-mode approach is adopted, accor ding to which, pseudorandom along with determinis tic patterns are applied to the CUT for detecting the random-pattern-testable (easy-to-detect) and the ran dom-pattern-resistant (hard-to-detect) faults, respect tively. In some mixed-mode cases, the deterministic patterns are inserted among the pseudorandomones. The application of deterministic patterns to theCUT is performed by loading, at specific times during testing, new (pre-calculated) initial states (seeds) to the test pattern generator (TPG). These seeds will expand to deterministic test vectors as theTPG runs.The most acceptable and widely used TPGs, when a mix ed-mode approach is used, are LFSRs.

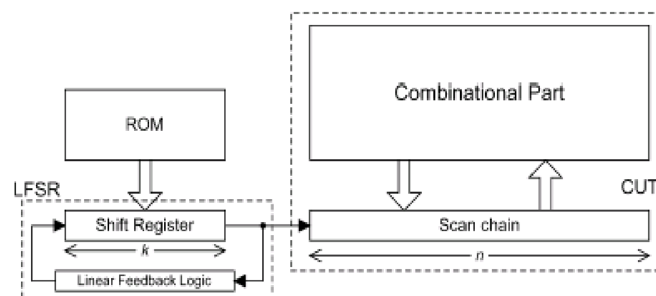


Fig. 1 Block Diagram

TEST PATTERN GENERATOR

It is a unit which is used for generating the test signals; this is done by three methods. They are Exhaustive / Pseudo Exhaustive Testing, Random Testing and Deterministic Testing.
It retains the advantages of exhaustive testing while significantly reducing the number of test patters to be applied. The basic idea is to partition the circuit under test into several sub circuits such that each sub circuit has a few enough inputs for exhaustive testing to be feasible for it. Traditional test generation techniques (Deterministic Test Patterns) may also be used to generate test patterns that can be applied to the circuit under test when it is in BIST mode. If the output response of the circuit under test do not match the expected response when the stored test patterns are applied in the presence of a fault. All though in principle this is a satisfactory approach for fault detection. This method is rarely used because of high overhead associated with storing test patterns and their responses.

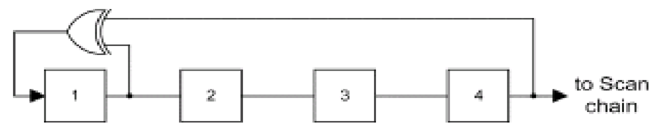


Fig: External-XOR LFSR with characteristic polynomial + + 1.

PROPOSED ARCHITECTURE

The overview of the proposed multiphase scan-based architecture is shown in Fig. The proposed scheme has two modes of operation: 1) the easy-fault-detection mode and 2) the hard-fault-detection mode. Although this distinction appears in every mixed-mode scheme, in the proposed one the operation of the scheme in these two modes differs significantly. During the easy-fault detection, the LFSR runs in autonomous mode and feeds the scan chain of the CUT from a single cell (the last one). The user defines the value of parameter *VectorsForEasyFaults*, which denotes the maximum number of vectors that can be used for detecting the easy faults. Only the Bit and Vector Counters are enabled during the easy-fault-detection mode. The Bit Counter controls the scan-in operation of each produced vector and signals the Vector Counter to increase, while the Vector Counter increases until a number of pseudorandom patterns equal to *VectorsForEasyFaults* have been applied to the CUT. The Reseeding and the Cell Selection Counters are initially reset like the Bit and Vector Counters, but they retain their initial zero value throughout the easy-fault-detection mode (i.e., they are disabled). The scheme's operation switches from the easy-vault-detection mode to the hard-fault-detection one when *VectorsForEasyFaults* pseudorandom patterns have been applied to the CUT, that is when Vector Counter reaches value *VectorsForEasyFaults*-1. For better explaining the proposed architecture's operation

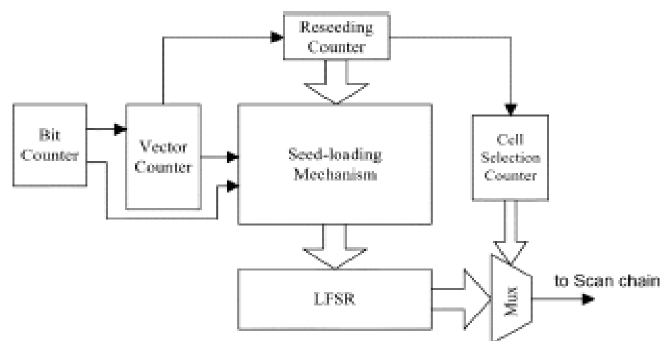


Fig. 3 Proposed Architecture

Let us now describe the operation of the proposed architecture in the hard-fault-detection mode more thoroughly. To simplify the description, we have omitted the capture cycle required after a test vector has been shifted in the scan chain. As we previously mentioned, at the end of the easy-fault-detection mode, Vector Counter's value is equal to *VectorsForEasyFaults*-1, while the Reseeding and the Cell Selection Counters are equal to 0 (Bit Counter's value is , where is the scan chain length). In the next clock edge, the first Reseeding is performed. TheVector Counter signals the Reseeding Counter to increase by one and *VectorsPerSeed* test vectors are about to be generated, starting from the seed that has been loaded in the LFSR. A new Reseeding is performed when the Vector Counter has counted *VectorsPerSeed* patterns and, of course, Bit Counter's value is (which means that the last test vector of the previous seed has been loaded in the scan chain). We note that when

performing a reseeding, Vector Counter's value is properly reduced, so as after the application of the *VectorsPerSeed* patterns of the new seed, to be equal to *VectorsForEasyFaults*-1. This way the only value of the Vector Counter that needs to be checked in all reseedings is *VectorsForEasyFaults*-1. When all the reseedings of a phase have been performed, the Reseeding Counter signals the Cell Selection Counter to increase and the next phase is initiated (Seed 1 is reloaded in the LFSR). The value of the Cell Selection Counter is increased by one at each new phase, thus enabling a different LFSR cell to feed the scan chain through the multiplexer. As for the Seed-loading Mechanism, it can be a ROM as in the classical reseeding approach, a combinational logic for reducing the hardware requirements of the BIST circuitry as will be described in Section
VII or it can even be eliminated and replaced by an external tester in a test resource partitioning scenario. This paper presents a new RF built-in self-test (BIST) measurement and a new automatic-performance-compensation network for a system-on-chip (SoC) transceiver. We built a 5-GHz low noise amplifier (LNA) with an on-chip BIST circuit using 0.18-μm SiGe technology. The BIST-measurement circuit contains a test amplifier and RF peak detectors. The complete measurement setup contains an LNA with a BIST circuit, an external RF source, RF relays, 50-Ω load impedance, and a dc voltmeter. The proposed BIST circuit measures input impedance, gain, noise figure, input return loss, and output signal-to-noise ratio of the LNA. The test technique utilizes the output dc-voltage measurements, and these measured values are translated to the LNA specifications such as the gain through the developed equations. The performance of the LNA was improved by using the new automatic compensation network (ACN) that adjusts the performance of the LNA with the processor in the SoC transceiver.
In this paper, a BIST technique for an RF transceiver front-end is presented. The test is aimed at spot defects typical of mass production in the CMOS process. The loop-back approach is used to detect faults modeled as resistive breaks or bridges. The resulting impairment in gain, noise figure or selectivity of the RF blocks are considered functional-level faults, and as such are subjected to test with PRBS stimulus and BER as the response at base-band. The extra test circuitry is limited and the on-chip resources are used to set-up the BiST. A model of a GSM transceiver with BiST is investigated to verify the proposed approach.

RF frequency synthesizers and transmitters for wireless system-on-chips have recently migrated to low-cost deep-submicrometer CMOS processes that facilitate all-digital implementations. In addition to all the benefits of lower power, lower silicon cost, reduced board area, and improved performance that the scaled CMOS integration entails, the testing costs for RF performance and wireless standard compliance could also be drastically reduced. In this brief, we propose a built-in self test (BIST) method, which is based on the premise that the internal frequency synthesizer and transmitter signals are in digital format allowing for digital signal processing to ascertain the RF performance without external test equipment. With the RF BIST capability, millions of SoCs can be calibrated and tested in a production environment using a low cost digital tester while benefiting from increased test coverage and reduced test time and cost. The presented techniques have been successfully implemented in two generations of commercial digital RF processors: 130-nm Bluetooth and 90-nm GSM single-chip radios

This paper addresses a built-in self-test (BiST) for Ics digital transceivers. The focus is on testing the RF frontend while taking advantage of the on-chip DSP resources and DA-, AD converters. The loopback architecture is used to prevent the sensitive RF blocks from extra noise and external disturbances. The test aims at spot defects typical of RF CMOS ICs, where those faults are deemed the main yield limiter in mass production. The fault model is discussed at three levels of design abstraction: layout, circuit and functional block.

The BiST model is verified at the circuit and functional level. As a demonstrator a GSM transceiver model with loopback BiST is presented that provides a promising result.

RESEEDING ALGORITHM:

In this section, we present an efficient algorithm for selecting the seeds and the LFSR cells, which will feed the scan chain of the CUT throughout testing. The main goal of this algorithm is to minimize the number of seeds required for fully (100%) testing the CUT. This way, the hardware required for the implementation of the proposed scheme will be minimized as well. The reseeding algorithm consists of three parts: 1) the easyfault- detection part, which is then followed by some test-cube preprocessing steps; 2) the seed and cell-selection part for detecting the hard faults; and 3) the test sequence-reduction part.

Easy-Fault Detection and Preprocessing:

The first part of the proposed algorithm is rather straightforward. The user defines the value of parameter *VectorsForEasy- Faults* as mentioned above, the LFSR is set to a random initial state and *VectorsForEasyFaults* random patterns are applied the CUT from the last LFSR cell, for testing the easy-to-detect faults. This pseudorandom part of the test sequence detects the vast majority of the faults of the CUT. The remaining faults are identified as hard-to-detect and multiple test cubes are extracted for each one of them by using the ATALANTA ATPG tool. Only a small subset of the extracted test cubes is selected for participating in the second part of the algorithm. This subset detects all hard faults and has much smaller cardinality than the initial test-cube set. The selection procedure (fault-simulation preprocessing) is fairly fast and targets both the optimization of the seed volume results and the run-time reduction of the second and main part of the reseeding algorithm.

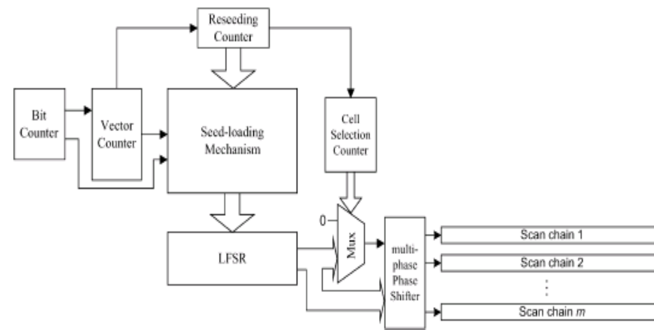
Selection of Seeds and LFSR Cells for Testing the Hard-to-Detect Faults :

The procedure that will be described in this section determines a seed and some LFSR cells for feeding the scan chain of the CUT in order to detect as many hard faults as possible. By repeating the same procedure we derive the final set of seeds and LFSR cells that will be used by the multiphase TPG. The seed-selection algorithm that will be presented tries to encode as many test cubes as possible to just one seed by exploiting the bit sequences produced by more than one cells of the LFSR. Before proceeding to the description of the algorithm, we should note that although the proposed TPG architecture performs all the reseedings while feeding the scan chain from the same LFSR cell (Fig. 6), the seed-selection algorithm examines the sequence of all LFSR cells when deciding for a new seed. That is, in order to preserve the regularity of the proposed architecture, the test vectors are applied to the CUT in different order from which they have been processed. This regularity is vital in the case that the Seed-loading Mechanism is implemented as combinational logic.

Test Sequence Reduction Procedure:

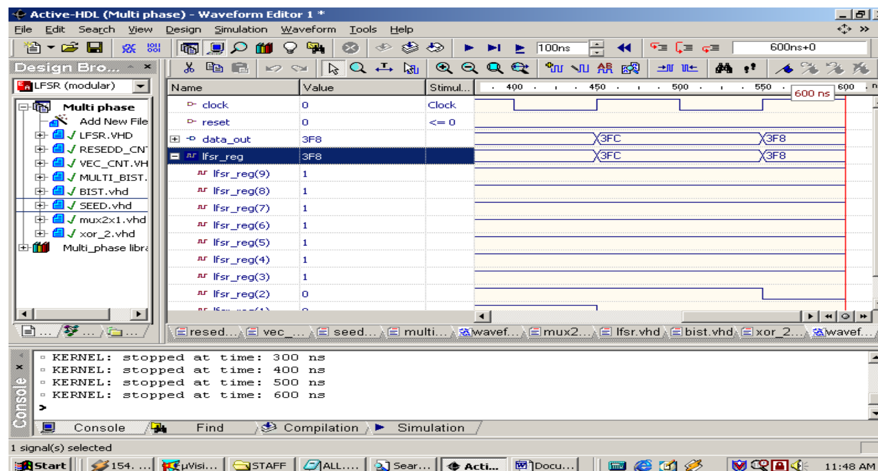
When all the necessary seeds and the cells of the LFSR that will feed the scan chain of the CUT have been determined, the third and final part of the reseeding algorithm is applied. This part attempts to reduce the test sequence length. Let us assume that:
1) LFSR cells have been selected for finally feeding the scan chain of the CUT (includes the last cell used in easy-fault-detection mode). 2) reseedings are performed. Then, the test sequence length, is equal to Test Sequence Length,

Test Sequence Length = Vectors For Easy Faults + P. R . Vectors Per Second.



The optimization procedure attempts to reduce each one of these factors in three steps, by fault simulating the vectors of the test sequence in various permutations.

Simulation Diagram:



APPLICATION OF THE MULTIPHASE TECHNIQUE TO MULTIPLE SCAN CHAIN ARCHITECTURES:

Multiphase Architecture for Multiple Scan Chains:

The main difference from the architecture proposed for a CUT with a single scan chain, is the multiphase Phase Shifter module, which is inserted between the multiplexer and the scan chains. The purpose of this module is twofold: it minimizes the linear dependencies among the bit sequences shifted in the scan chains, as well as, by receiving the output of the multiplexer, it feeds the scan chains of the CUT with different shifted versions of the LFSR's -sequence.

Reseeding Algorithm in the Multiple Scan Chain Case:

Handling the additional constant 0 value of the multiplexer is what differentiates the reseeding algorithm for the multiple scan chain case from that for the single one. As

explained above, the constant 0 value is used in the easy-fault-detection mode and is also considered during seed selection. That is, it is utilized exactly as the preselected last LFSR cell in the single scan chain case. So, when a number of LFSR cells has been selected by the reseeding algorithm, one of them (the first one) corresponds to the constant 0 value

Dynamic Reseeding:

The dynamic reseeding scheme along with the counters of the multiphase architecture that control it. The reseeding operation is performed by inverting, at certain clock cycles, the outputs of some of the LFSR cells before being stored to their adjacent cells. This is achieved by means of additional XOR gates, which are placed between the cells of the LFSR. When the Multiphase Architecture is implemented using the Dynamic Reseeding Scheme, the Seed loading Mechanism of the former is compromised of the Inversion Control Module and the additional XOR gates.

CONCLUSION

We have described a novel multiphase reseeding architecture for scan-based BIST. Multiple cells of the LFSR, which are used as TPG, feed the scan chain of the CUT in different test phases. Since the operation of the LFSR is identical in all of them, i.e., the LFSR passes through the same state sequence, the implementation cost of the proposed architecture remains low. Furthermore, the encoding ability of an LFSR seed is enhanced
When the bit sequences generated by more than one LFSR cells are considered during its calculation. Thus, the reseeding algorithm that accompanies the multiphase architecture manages to reduce the number of necessary seeds for fully testing the CUT significantly, compared to the already known reseeding techniques. As a result, the proposed architecture is suitable when either a full BIST or a test resource partitioning approach is selected. When BIST is the desired solution, the designer can choose between the flexibility that an on-chip ROM offers and the area gain that can be achieved when the proposed architecture is combined with the dynamic reseeding scheme.

This paper introduces a novel architecture that is targeted for digital core testing and built-in-self test (BIST) algorithm development. This reconfigurable architecture is validated by an application that implements the novel idea of verifying algorithms for testing digital circuits by using runtime reconfigurable techniques in order to minimize the circuit area, as well as the test generation and application time. The idea revolves around the dynamic partial reconfiguration of circuits under test in order to inject stuck-at faults at different locations of the circuit and uncover both detectable and undetectable faults. Four testing strategies are presented, and two are experimentally compared, namely, the sequential compile-time reconfiguration and runtime reconfiguration strategies.

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