Low power VLSI architecture for adaptive filter and its application to noise cancellation

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ABSTRACT

Here we present an architectural approach to design an adaptive filter with low power consumption. The proposed architecture is efficient in achieving less power consumption without degrading the filter performance. Basically, an adaptive filter comprises of a variable filter and a filter coefficient updating algorithm. The variable filter is an FIR filter due to its stability, which has larger amplitude variations in input data and filter coefficients. As filtering part is the major contributor of power in an adaptive system, cancellation of unwanted multiplications by considering these amplitude differences will cause a significant reduction in power. The order of the variable filter is also changed dynamically because the power is reduced by turning off some of the multipliers based on the amplitude of input data and filter coefficient. To perform the adaptation process, that is convergence of output computed by the variable low power FIR filter to a desirable output an LMS algorithm is used. As one of the important applications of adaptive filtering, noise cancellation is performed on a signal with injected noise. The low power adaptive filter architecture is VHDL coded and simulated on ModelSim to check the desired functionality. Then the filter design is synthesized on Xilinx ISE suit for generating power report. Experimental results show significant reduction in power without compromising filter performance and also less area overhead is identified from the synthesis report.

Key words: Approximate filtering, low power filter, reconfigurable design, low power digital signal processing, adaptive noise cancellation.

INTRODUCTION

Real-world signals which are analog in nature need to be processed so that the information contained in them can be displayed, analyzed or converted to other useful form, which is performed by a Digital Signal Processing (DSP) system. Digital Signal Processing has been executing a major role in the current technical advancements such as noise cancellation, echo cancellation, voice prediction etc. So, for obtaining quick and acceptable solutions for these problems adaptive filtering techniques must be implemented other than standard DSP techniques. In general, filtering is one of the widely used operations in Digital Signal Processing (DSP). A filter is a signal selection system that is used to extract desired signal from a noisy signal which consists of disturbances, whereas adaptive filter is particularly useful whenever the statistics of the input signals to the filter are unknown or time varying

and the design requirements for fixed filters cannot easily be specified. The basic operation of adaptive filter involves two processes: a filtering process and an adaptation process. The filtering process is usually FIR filtering due to stability measures. The adaptation process uses an adaptation algorithm to update the filter coefficients according to the working environment. As Filters are one of the major determinants of performance and power consumption of the whole system, there is an increased concern for designing low power filter structures. As the paper aims to design a low power FIR adaptive filter, a summary of earlier efforts on reducing power consumption of FIR filter is discussed below.

Several works on lowering power consumptions of FIR filters have been proposed earlier. Some previous works have tried to optimize the filter coefficient while maintaining fixed filter order. In those approaches, filter structures are simplified to add and shift operations and the power reduction is achieved by minimizing number of additions. However, one of the major drawbacks of such approaches is that the coefficient cannot be changed, once the filter order is fixed. There for those techniques are not applicable to the FIR filters with programmable coefficients. For the design of low power FIR filters, approximate signal processing techniques [10] has also been used. In energy scalable system design [9], it is shown that sorting the data samples and coefficients before convolution operation has some energy quality characteristics. In this approach, for desirable energy quality behaviour of FIR filter, MAC cycles that contribute significantly to the filter output is accumulated first by sorting. However, the overhead due to the real-time sorting of data samples is too large. In [6], a modified distributed algorithm (DA) for low power finite impulse response filter has been proposed. Several reconfigurable low power filter architectures have also been proposed. [5] Presented a low power FIR filter architecture with variable input word length and filter taps. It provides flexible, compact and low power solutions to FIR filters with wide range of precision and tap lengths. But there is a large overhead due to arbitrary non-zero digit assignment. Reconfigurable architectures with different word length filter coefficients [2] for low power applications have been proposed. Similar to other reconfigurable architectures, large overhead is incurred due to programmable shift.

This paper presents low power architecture for adaptive filter. The proposed adaptive system consists of a reconfigurable and low power FIR filter for filtering process and LMS algorithm for the adaptation process. The low power and reconfigurable FIR filter achieves lower dynamic power consumption by cancelling unwanted multiplications. The resulting error is being controlled by keeping it as small as the quantization error, which in turn minimizes the filter performance degradation. Even though, several algorithms are available for adaptation process, LMS is used here because of its low complexity and proven robustness.

ARCHITECTURE OF LOW POWER ADAPTIVE FILTER

Adaptive filter is an attractive technique for real-time applications where there is no time for statistical estimation and for application with non-stationary signals. These filters operate satisfactorily in unknown and time varying environments without user interventions. The general block diagram of an adaptive filter is given in Figure 1. Adaptive filters are composed of three basic modules such as filtering structure, performance criterion and adaptive algorithm. The filtering structure determines the output of the filter from given input samples. FIR is preferred over the IIR for filtering due to stability measures. Then, the performance criterion is chosen according to the application and it is used to derive the adaptive algorithm.

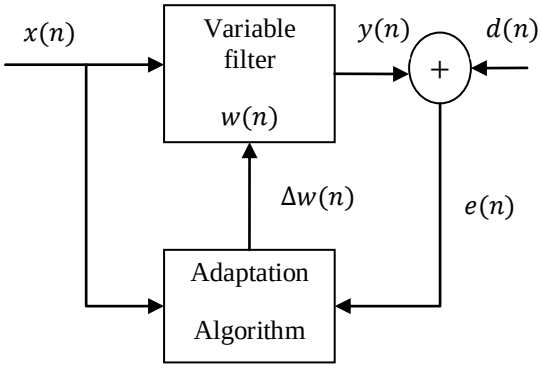

Fig 1: General block diagram of adaptive filter

The three generally used performance criteria are mean squared error, least squares and weighted least squares. Finally, the adaptive algorithm is used to update the filter coefficient based on the performance criterion to improve the performance. The low power adaptive filter as shown in figure.2 consists of a low power and reconfigurable FIR filter for filtering process and LMS algorithm for adaptation process. Here the performance criterion based on which LMS algorithm update filter coefficients is mean square error value.

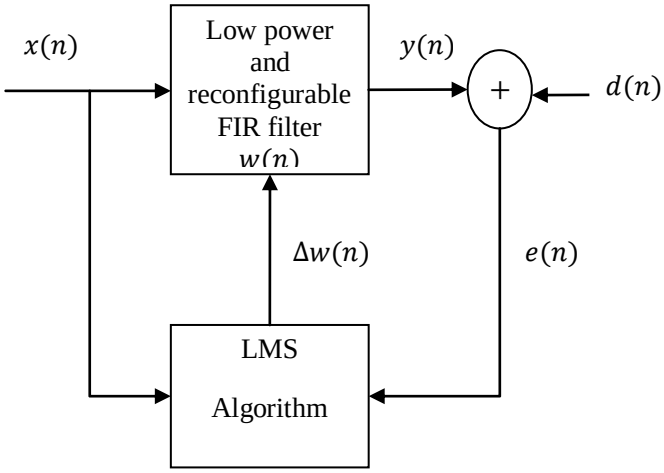

Fig 2: Block diagram of low power adaptive filter

Reconfigurable FIR filter architecture

Finite Impulse Response (FIR) filtering is one of the widely used operations in DSP. The output of the FIR filter is the weighted sum of current and finite number of previous input samples called convolution. The direct form architecture of FIR filter is shown in Figure 3. Linear phase characteristics, inherent stability and requires no feedback are the main advantages of a FIR filter. Its main disadvantage is large computational power as compared to IIR filter. The output $y[n]$ of a linear time invariant FIR filter is given by the following equation.

$$y[n] = \sum_{i=0}^{N} c_i \, x[n-i] \quad (1)$$

In general, for a FIR filter the power consumption is directly proportional to the amount of computation. To reduce the power consumption, the proposed FIR filter structure cancels unwanted multiplications. The architecture is reconfigurable because it changes the filter order dynamically by considering the amplitude of data samples and filter coefficients. The performance of the filter is still maintained by making the product of data sample and the filter coefficient as small as the quantization error.

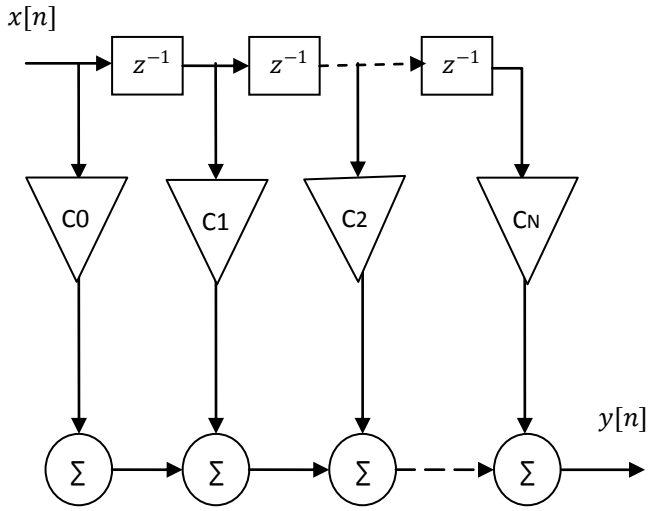

Fig 3: Direct form architecture of conventional FIR filter

Figure.4 shows the architecture of reconfigurable FIR filter. It consists of three main sections. Amplitude Detector (AD), Multiplier Control Signal Decision window (MCSD) and a control signal generator. The architecture reduces the power consumption by switching off some of the multipliers based on the amplitude. More specifically, the dynamic power is reduced because the switching activity of internal node capacitance directly contributes to the total dynamic power consumption of a CMOS gate.

As specified earlier, the proposed reconfigurable architecture dynamically changes the filter order when multipliers get turned off based on the filter coefficient and data sample amplitudes. The criterion for cancelling the multiplications is that the amplitude of both data sample and filter coefficient is less that predetermined threshold value or not. For checking this criterion a combinational logic circuit called Amplitude Detector (AD) is used. If the amplitude of the incoming data sample is smaller than the threshold (x_{th})., the output of AD (ad_out) becomes "1". One problem that occurs while using this logic is that, if the amplitude of the input data samples changes abruptly for every cycle, then the multipliers will be turned off and on continuously. This in turn increases the switching activity and thus the dynamic power increases. To solve this switching problem Multiplier Control Signal Decision window (MCSD) is used which is explained in the following section. For the low power adaptive filter, AD is required for each filter coefficient as the amplitude of the coefficient is varying. The amplitude detector for each filter co-efficient compares the amplitude of the coefficient with a predetermined threshold value(c_{th}) and if it is smaller, then the output (ad_coeff) becomes "1".

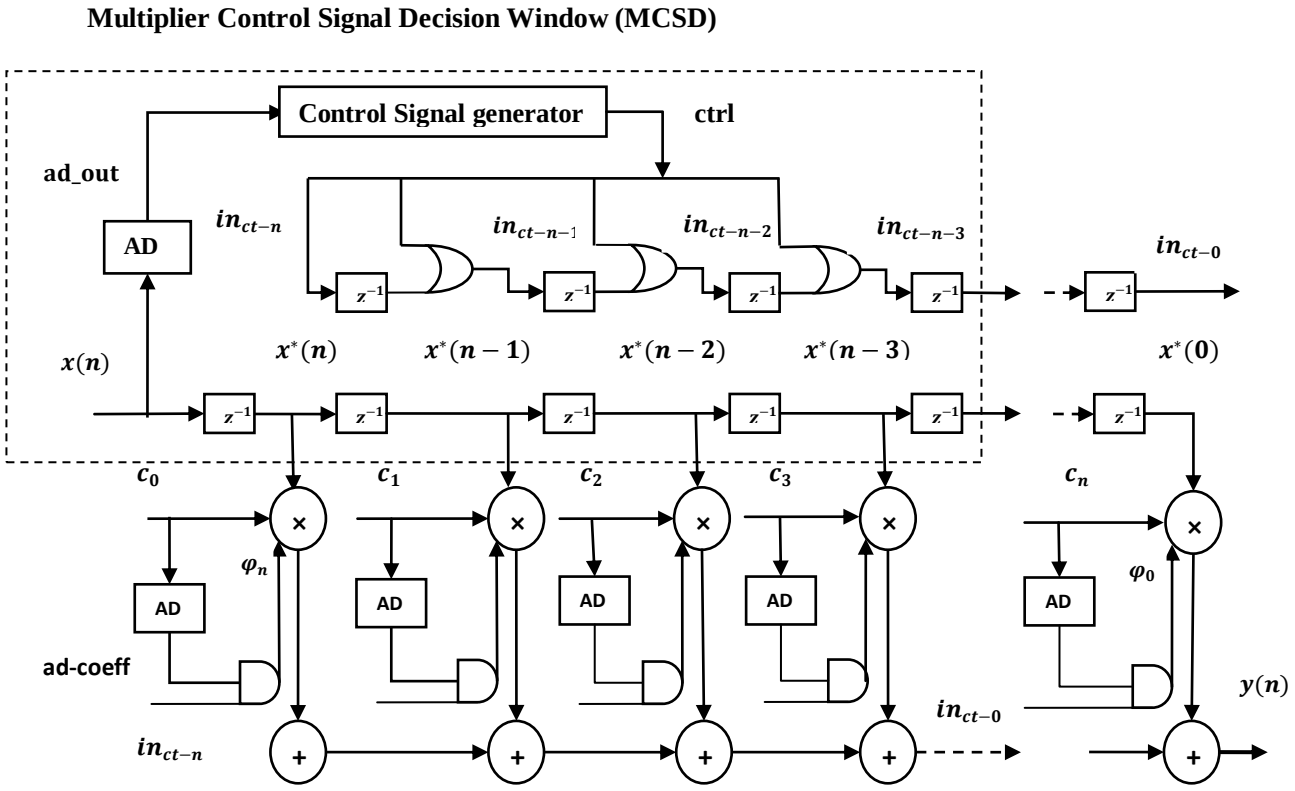

Fig 4: Architecture of Reconfigurable FIR filter

Multiplier Control Signal Decision window (MCSD) is used to reduce the frequency of switching activity. There is a control signal generator within the MCSD window which reduces the switching problem. The control signal generator consists of an internal counter which counts the number of input samples for which the condition $x[n] < x_{th}$ is satisfied. That is, the counter starts counting up whenever the output of the amplitude detector (ad_out) is set to "1". When the count reaches certain value (*say m*), the output of the control signal generator (ctrl) becomes "1", where *m* is the size of MCSD .So, a "1" value on *ctrl* is an indication that m consecutive small inputs are monitored and multipliers are ready to turn off. The signal *ctrl* also controls an additional signal in_{ct-n}. This signal accompanies with the input data all the way in the following flip flops to indicate that $x[n] < x_{th}$, and the multiplications can be cancelled if the corresponding filter coefficient amplitude is smaller than c_{th}. In figure 4, an additional delay element is added before the first tap to synchronize in_{ct-n} and $x^*(n)$. The procedure of turning off the multiplier after getting the filter coefficient and data sample smaller than the corresponding threshold is as follows. When the amplitude of the input data sample and filter coefficient is smaller than the thresholds, the signal φ_n is set to "1". Whenever the signal φ_n is set to logic "1", the multiplier will be turned off by a simple logic circuit and the output in turn forced to zero.

An important thing to consider while designing the reconfigurable filter section is the values for the threshold x_{th} and c_{th} , which has a significant impact on the filter performance and power consumption. If the threshold values are very large, it can give rise to large power savings at the cost of filter performance. On the other hand if the threshold values are small, then the power savings become trivial. Similarly the values of$m$, indicating the size of MCSD also have significant impact on the power savings. So, if m becomes larger, then the

number of input samples that makes multipliers turned off decreases. Then the power reduction becomes smaller and filter performance degradation becomes lower as well.

The Adaptation Algorithm

The adaptive filter computes the output signal of the filter, and compares it to a desired output signal dictated by the true system. Then the error signal which is the difference between the desired and estimated output signal is used as objective function in mean square sense. The filter tap weights are then changed so that the error signal is minimized to improve the performance. The adaptation process that is convergence of estimated filter output to desired filter output by minimizing the error signal is performed by the adaptation algorithm. There are several adaptation algorithms with different performance criterion. Due to its low complexity and proven robustness, Least Mean Square (LMS) algorithm is used here. LMS algorithm is a noisy approximation of steepest descent algorithm. It is a gradient-type algorithm that updates the coefficient vector by taking a step in the direction of the negative gradient of the objective function.

$$w(n+1) \quad = w(k) - \frac{\mu}{2} \frac{\partial J\mathbf{w}}{\partial w\,(n)} \tag{2}$$

where μ, is the step size controlling the stability, convergence speed and misadjustment. To find an estimate of the gradient, the LMS algorithm uses an objective function considered as the instantaneous estimate of the mean square error, i.e., $J\mathbf{w} = e^2(n)$ resulting in the gradient estimate $\partial J\mathbf{w}/\,\partial w(\mathrm{n}) = -2e(n)\,x(n)$. In order to guarantee stability in the mean-squared sense, the step size μ should be chosen in the range $0 < \mu < 2/\mathrm{tr}\{\mathrm{R}\}$, where tr {R.} is the trace operator and the input-signal autocorrelation matrix is given by

$$R = E[x(n)x^T(n)] \tag{3}$$

Table1. The Least Mean Square Algorithm

LMS Algorithm

For each n
{
y(n) = w^T (n)x(n)
 	
e(n) = d(n) – y(n)
 	
w(n+1) = w(n) + μe(n)x(n)
}

The mathematical model of LMS adaptive filter is given in Table1. As discussed earlier, the LMS algorithm update the filter coefficient for tracking the desired filter output using the error signal (*e(n)*). In the mathematical model, y*(n)* is the computed filter output, $w^T(n)$ is the filter coefficients in transposed form, *x(n)* is the filter input samples, *e(n)* is the error signal which used for updating the filter coefficients and μ is the step size or the learning factor. Figure.5 shows the general direct form LMS adaptive filter structure for updating filter tap weights. The filter tap weights are updated using the equation $w(n+1) = w(n) + \mu e(n)x(n)$, ie., the new filter tap weights are generated from the current tap weight based on the step size, error signal.

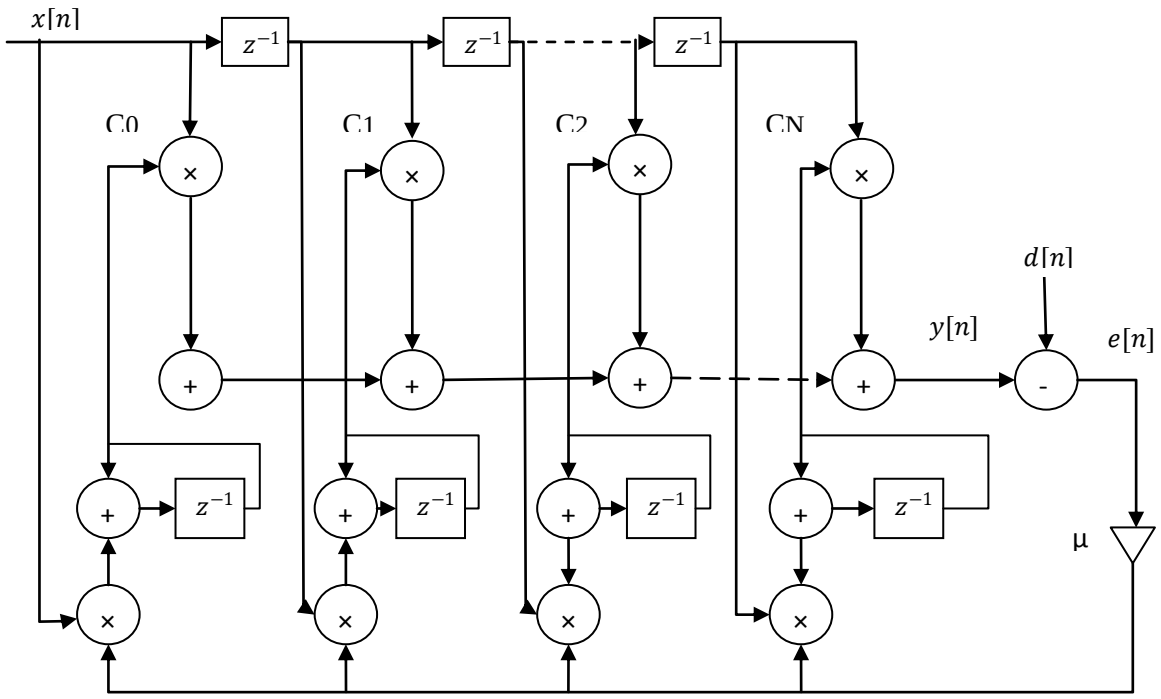

Fig 5: Direct form LMS adaptive filter structure (Conventional)

ADAPTIVE NOISE CANCELLATION

Adaptive filtering technique is suitable for applications in which the statistics of the input is unknown or time varying. Examples of such applications are Noise cancellation, System identification, voice prediction, acoustic echo cancellation. Here we are considering the low power adaptive filtering application to noise cancellation in detail. Figure.6 shows the low power adaptive noise cancellation configuration. For demonstrating the noise cancellation application using adaptive filtering, we have taken a noisy signal as the filter input which is given as $x(n) = N_1(n)$. The filter part of the adaptive system computes the output $y(n)$ from the noisy input signal $N_1(n)$. The noisy output $y(n)$ is then compared with the desired signal $d(n)$. The desired signal $d(n)$ consists of a signal $s(n)$ corrupted by another noise $N_0(n)$. Now the adaptive algorithm updates the filter coefficients to cause the error signal $e(n)$ to be the noiseless version of $s(n)$.

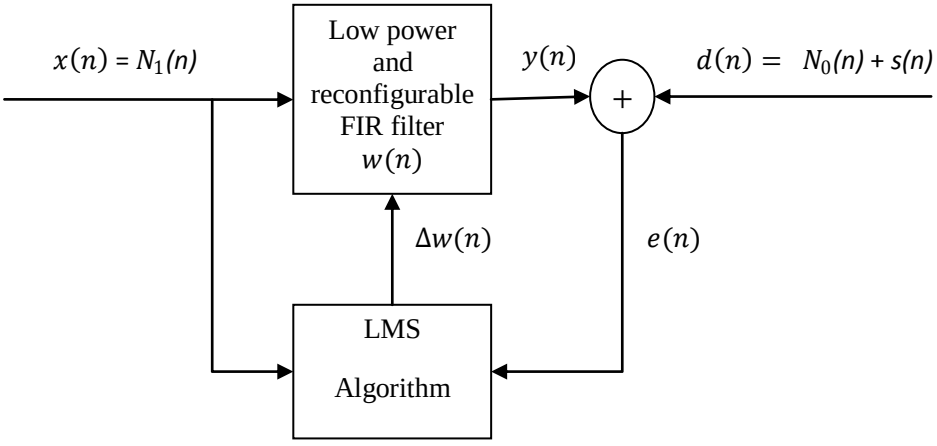

Fig 6: Adaptive noise cancellation configuration

One important thing to consider is that both the noise signals used for this configuration must be uncorrelated to the signal *s(n)*. While performing the adaptation process, the error signal will never become zero, which means the configuration will only minimize the difference between the two signals.

RESULTS AND DISCUSSIONS

The low power adaptive filter is VHDL coded and simulated on ModelSim to check the desired functionality. The filter specifications are 8 bit data samples, 8 bit filter coefficients and 4 bit threshold for both input data and filter coefficients. For comparison we have VHDL coded the conventional filter structures. Figure.7 and Figure.8 shows the ModelSim snapshots of conventional and reconfigurable FIR filter. The simulation results of conventional and low power adaptive filter is shown in Figure.9 and Figure.10. The filter structured in VHDL is synthesized on Xilinx ISE. The Xpower analysis on Xilinx provides the power report. The power report of low power adaptive filter shows a power reduction of 25% from the conventional filter at a clock frequency of 100 MHz.

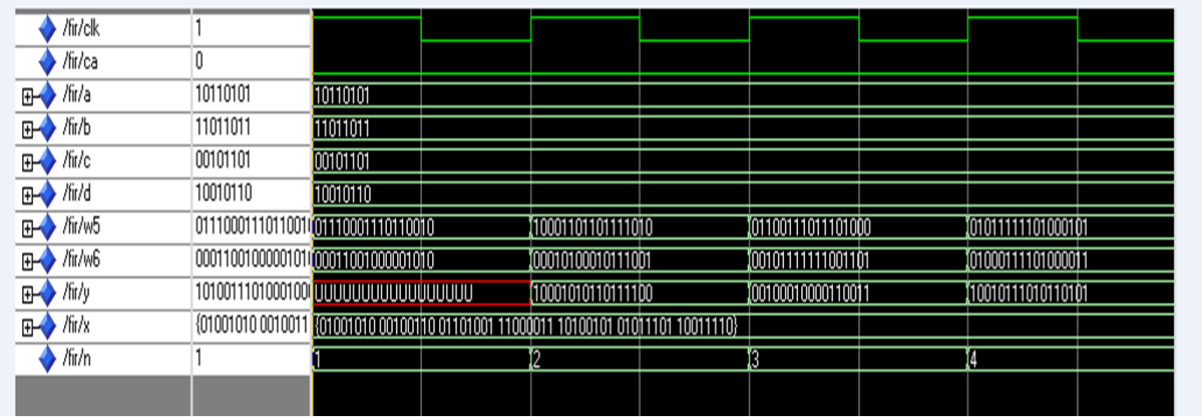

Fig 7: Simulation result of conventional FIR filter.

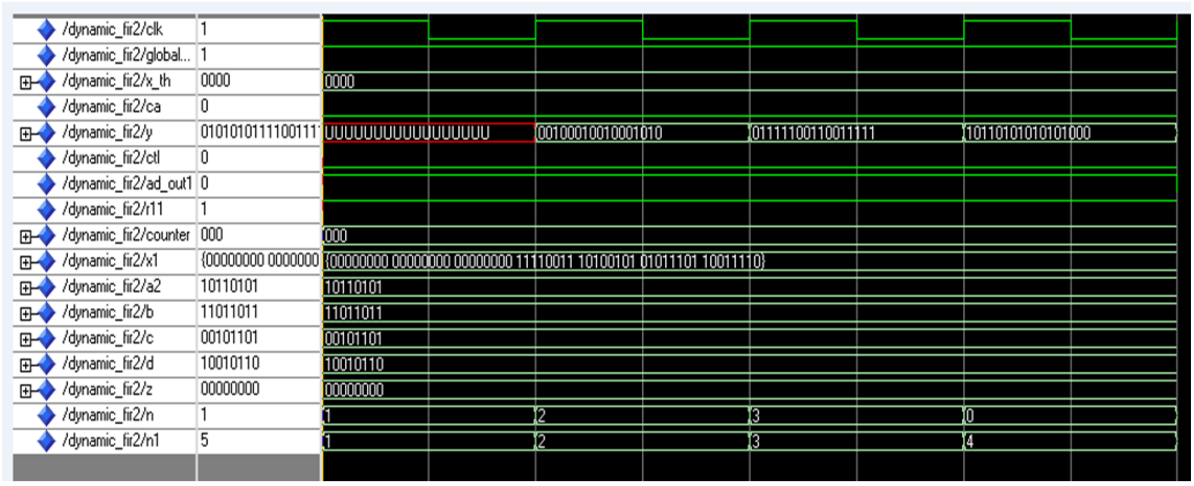

Fig 8: Simulation result of reconfigurable FIR filter

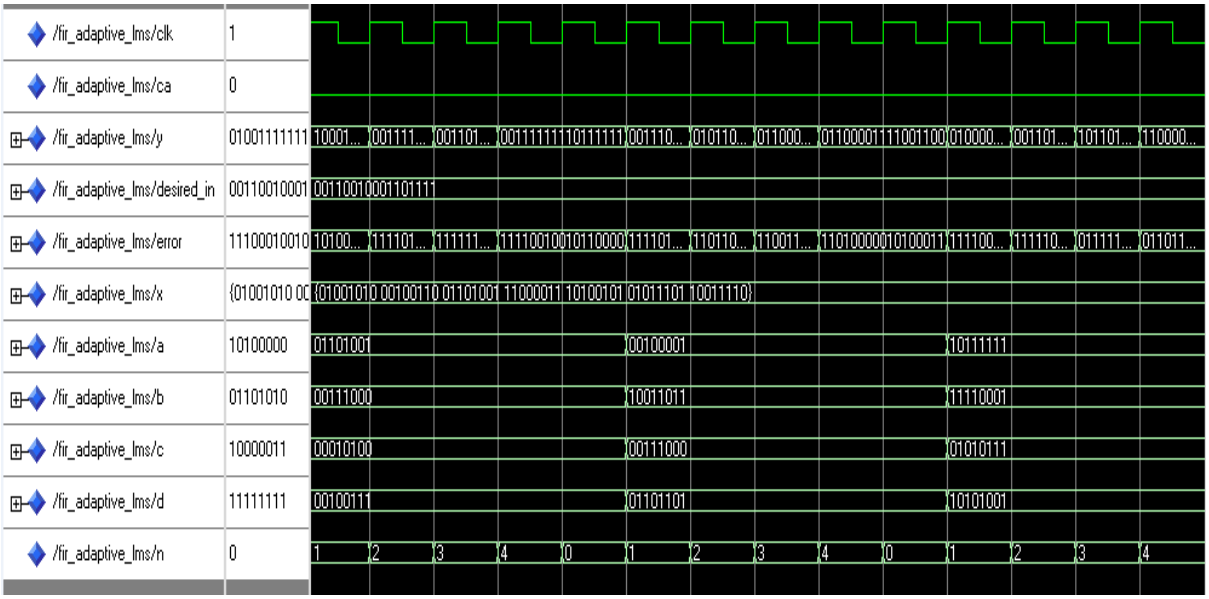

Fig 9: Simulation result of conventional adaptive filter

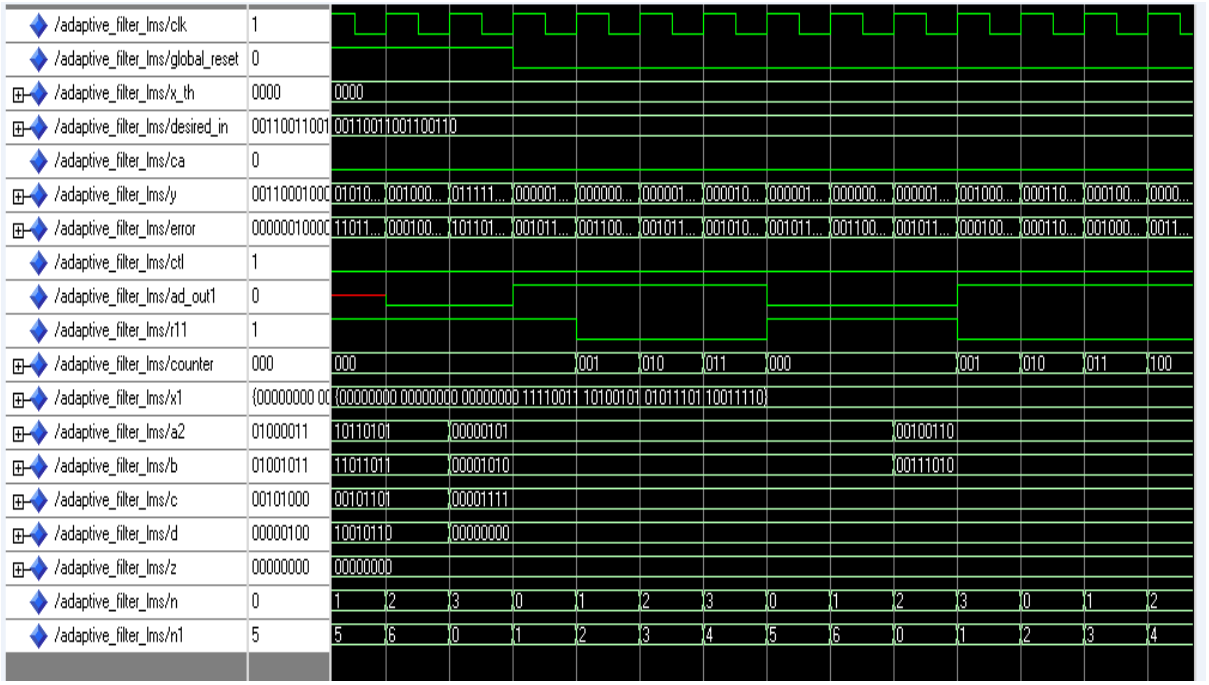

Fig 10: Simulation result of low power adaptive filter

The low power adaptive configuration for noise cancellation is also VHDL coded and simulated on ModelSim. The filter specifications are 8 bit input data, 8 bit filter coefficients and 4 bit threshold as specified earlier. The signals $N_0(n)$ and $N_1(n)$ are not real-time signals, but both are injected noises in VHDL. In Figure.11 the signal *op* is the noisy signal and *op1* is the filtered noiseless signal after several iterations.

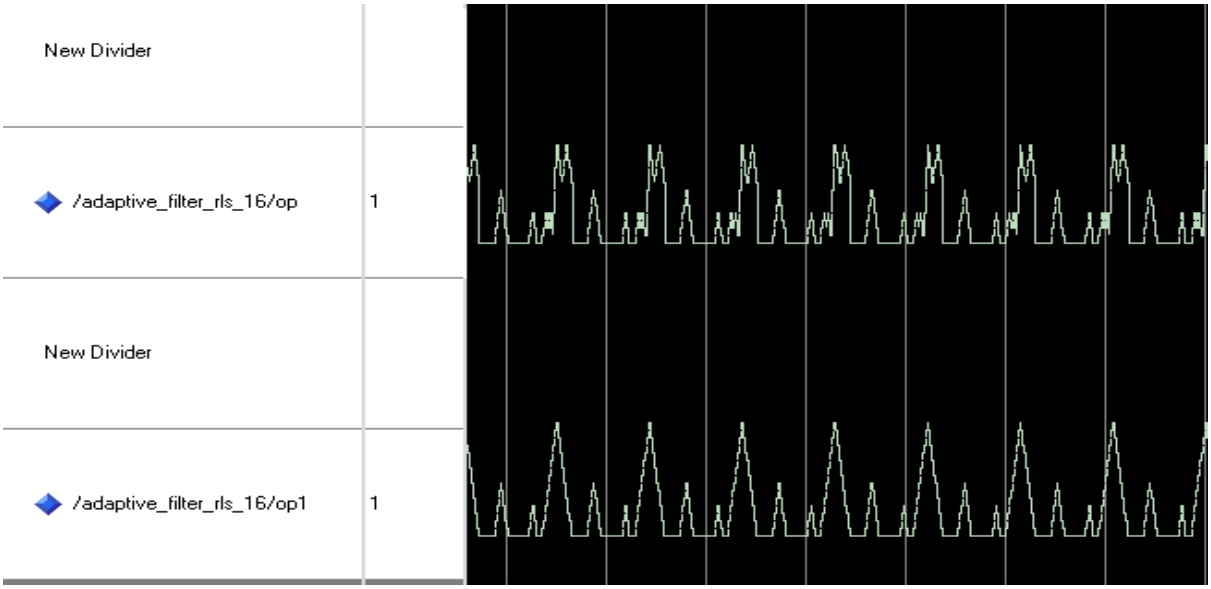

Fig 11: Simulation result of Low power adaptive noise cancellation filter

CONCLUSION

In this paper, low power architecture for adaptive filter is proposed. The low power adaptive filter consists of a reconfigurable low power FIR filter and the LMS algorithm. The amplitude of both data samples and filter coefficients are monitored by the reconfigurable FIR filter and the multipliers are turned off when the amplitudes are smaller than the predetermined threshold values. The LMS algorithm is used to update the transfer function of reconfigurable filter with low complexity. The experimental results showed significant reduction in power without degrading the filter performance. The application of low power adaptive filter to noise cancellation is demonstrated using a signal with injected noise. The simulation result showed that the proposed filter architecture removes the noise from the given noisy signal without casing much degradation to the original signal with less power consumption. The proposed low power adaptive filtering system can also be used for other applications such as system identification, echo cancellation etc.

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