DESIGN AND VERIFICATION OF ONLINE BIST FOR DIFFERENT WORD SIZES OF MEMORIES

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1. ABSTRACT

Transparent BIST schemes for RAM modules assure the preservation of memory contents during periodic testing. Symmetric Transparent Built in self test (BIST) schemes skip the signature prediction phase required in traditional transparent BIST, achieving considerable reduction in test time. Previous works on symmetric transparent BIST schemes require that a separate BIST module is utilized for each RAM under test. This approach, given the large number of memories available in current chips, increases the hardware overhead of the BIST circuitry.

In this work we propose a symmetric transparent BIST scheme that can be utilized to test RAMs of different word widths; hence, more than one RAM can be tested in a roving manner. The hardware overhead of the proposed scheme is considerably smaller compared to the utilization of previously proposed symmetric transparent schemes for typical memory configurations.
BIST(built in self test),dft(design for testability),

2. INTRODUCTION

This chapter introduces the basic theory behind memory testing. There are two kinds of memory test methods: electrical (technology-dependent) and functional (technology-independent). Electrical memory testing consists of parametric testing, which includes testing DC and AC parameters, IDDQ and dynamic testing for recovery, retention and imbalance faults. DC and AC parametric tests are used to verify that the device meets its specifications with regard to its electrical characteristics, such as voltage, current,and setup and hold time requirements of chip's pins. Since embedded memories in SOCs usually do not have their I/O ports directly connected to chip's pins, parametric testing for embedded memories is not a necessity. IDDQ and dynamic testing need a detailed description of the specific process technology. Additional information on electrical testing can be found in .This thesis focuses on technology-independent functional memory testing, whose purpose is to verify the logical behavior of a memory core. Because functional memory testing allows for the development of cost-effective short test algorithms (without requiring too much internal knowledge of the memory under test), it is widely accepted

by industry as a low-cost/high-quality solution. This chapter provides a theoretical background and explains the memory functional test models.

Most of the definitions and figures in this chapter are excerpted from BIST is a Design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary as widely as the product diversity that it caters to. As an example, a common BIST approach for DRAM's includes the incorporation onto the chip of additional circuits for pattern generation, timing, mode selection, and go-/no-go diagnostic tests.

The main drivers for the widespread development of BIST techniques are the fast-rising costs of ATE testing and the growing complexity of integrated circuits. It is now common to see complex devices that have functionally diverse blocks built on different technologies inside them. Such complex devices require high-end mixed-signal testers that possess special digital and analog testing capabilities. BIST can be used to perform these special tests with additional on-chip test circuits, eliminating the need to acquire such high-end testers.

BIST is also the solution to the testing of critical circuits that have no direct connections to external pins, such as embedded memories used internally by the devices. In the near future, even the most advanced tester may no longer be adequate for the fastest chip, a situation where in self-testing may be the best solution for.

Advantages of implementing BIST include: 1) lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated; 2) better fault coverage, since special test structures can be incorporated onto the chips; 3) shorter test times if the BIST can be designed to test more structures in parallel; 4) easier customer support; and 5) capability to perform tests outside the production electrical testing environment. The last advantage mentioned can actually allow the consumers themselves to test the chips prior to mounting or even after these are in the application boards.

Issues that need to be considered when implementing BIST are: 1) faults to be covered by the BIST and how these will be tested for; 2) how much chip area will be occupied by the BIST circuits; 3) external supply and excitation requirements of the BIST; 4) test time and effectiveness of the BIST; 5) flexibility and changeability of the BIST (i.e., can the BIST be reprogrammed through an on-chip ROM?); 6) how the BIST will impact the production electrical test processes that are already in place.

3. Implementation Methodology:

The drawbacks of existing system are, in transparent BIST the signature prediction phase adds the total testing time up to 30% and separate BIST modules are used for each RAM which increases the hardware overhead.

In transparent BIST the content of the memory at the end of the test is identical to before the test. Since the read elements of signature prediction phase is identical to the read elements of

the testing phase. But in my proposed work,more than one memory with varying word widths are used when the number of stages of the ALU is larger than the memory word width. The block diagram and flow diagram of the proposed methodology.

First, the number of bits in the RAM is initialized. Here, RAMs of different word widths are used. By creating the rules, the fault addresses are checked by using BIST. From that, row and column address information from BIST are predicted. These faulty addresses are copied to RAM arrays. The next block is March test. The test is marching through memory. From these, all these information are fed to solution stage by multiplexing all the address separate for rows and columns.

The next block is extract march bits. March 1 bit beginsby writing backgrounds of 0s then read an d write back complement values for all cells. Marching-0 follows exactly the same pattern, with the data reversed. The next block is checking error and finally each possible

Symmetric Transparent March c- algorithm:

	(a)	(b)	(c)
M_0.	$\Uparrow (w_0)$;	$\Uparrow (r_a)$; $\Uparrow ((r_a)^c)$; $\Downarrow (r_a)$; $\Downarrow ((r_a)^c)$; $\Downarrow (r_a)$;	$\Uparrow ((r_a)^c)$;
M_1.	$\Uparrow (r_0, w_1)$;	$\Uparrow (r_a, w_a^c)$;	$\Uparrow (r_a, w_a^c)$;
M_2.	$\Uparrow (r_1, w_0)$;	$\Uparrow (r_a^c, w_a)$;	$\Uparrow (r_a^c, w_a)$;
M_3.	$\Downarrow (r_0, w_1)$;	$\Downarrow (r_a, w_a^c)$;	$\Downarrow (r_a, w_a^c)$;
M4.	$\Downarrow (r_1, w_0)$;	$\Downarrow (r_a^c, w_a)$;	$\Downarrow (r_a^c, w_a)$;
M_5.	$\Downarrow (r_0)$;	$\Downarrow (r_a)$;	$\Downarrow (r_a)$;

Figure 1: C- march algorithm (a) original version (b) transparent version (c) symmetric transparent version

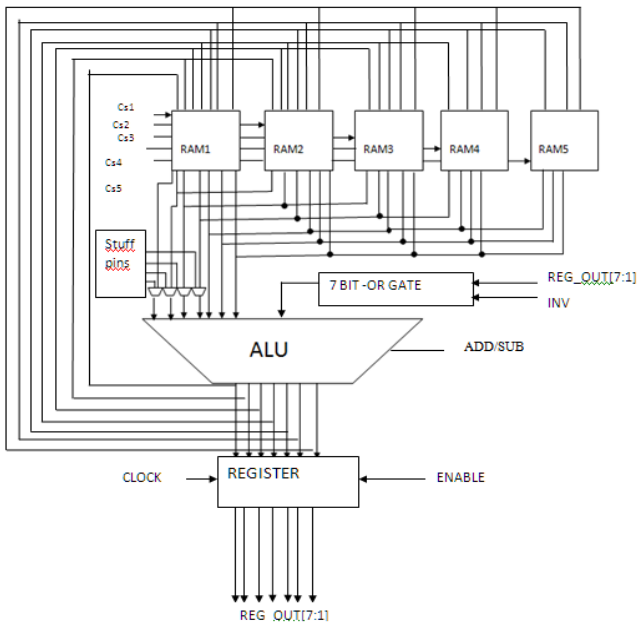

Fig: transparent testing of ram module with different word with

3.1 Transparent online BIST for an array of RAM modules:

For the case of three RAM modules, having different word width with 3, 4, 5, 6 and 7 bits each, are to be tested transparently online in a roaming manner using a 7 stage ALU. The RAM to be tested is enabled through the cs1,cs2,cs3,cs4 and cs5 chip select signal. When the RAM1 is tested, the inputs of the ALU are driven by the outputs of the RAM1; when RAM2 is tested, the higher order input of the ALU is driven by the stuff2 signal; when RAM3 is tested, the two high order inputs are driven by the signals stuff1 and stuff2, when RAM4 is tested the three high order inputs are driven by signals stuff1,stuff2 and stuff3,when RAM5 is tested the four high order inputs are driven by signals stuff1,stuff2,stuff3 and stuff4.

4. Experimental Results

RAM1 testing

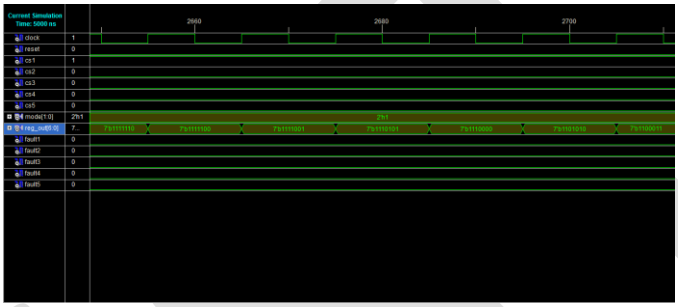

Fig.4.1

RAM2 testing

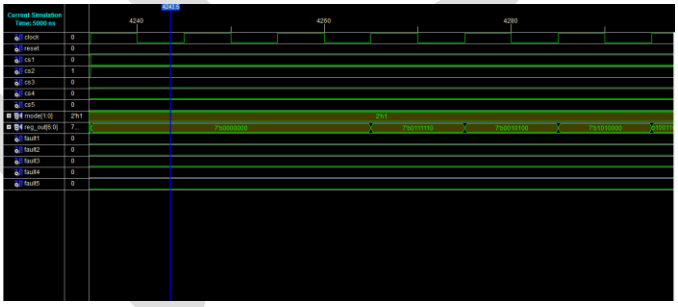

Fig.4.2

RAM3 testing

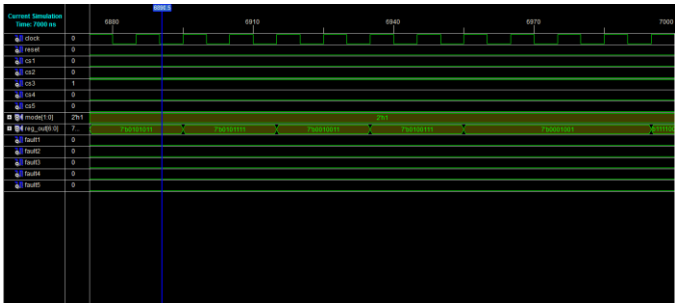

Fig.4.3

RAM4 testing

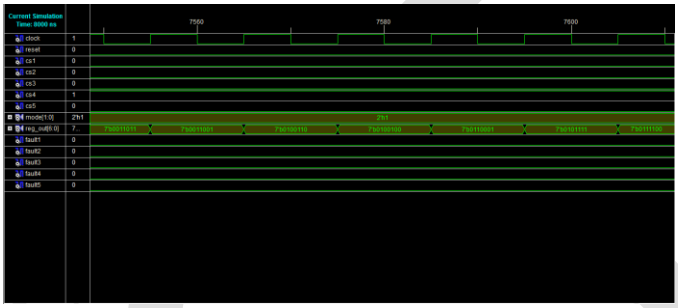

Fig:4.4

RAM5 testing

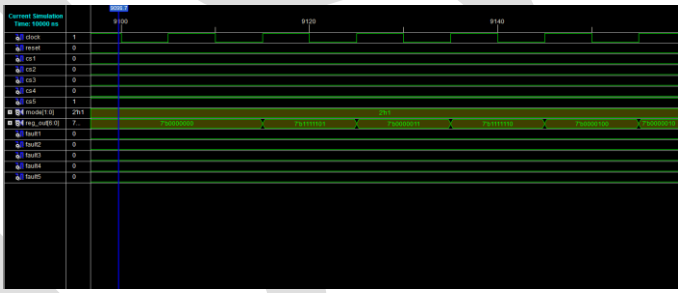

Fig:4.5

RTL schematic

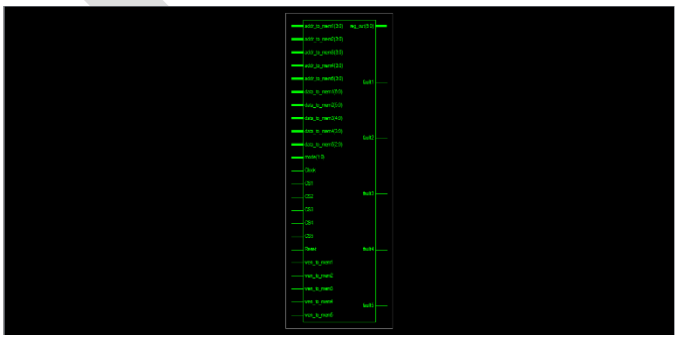

Fig.4.6

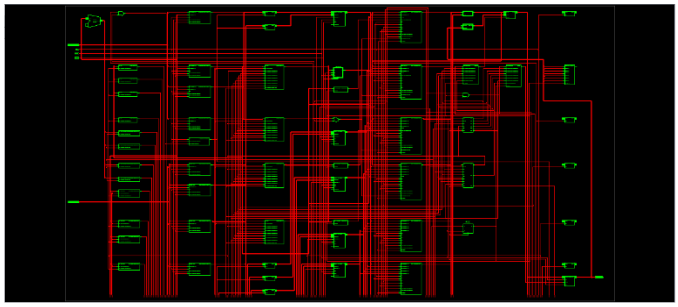

Fig.4.7

5. Conclusions

In this paper testing of RAM modules has been presented using the symmetric transparent principle. This scheme tests a RAM utilizing an ALU module whose number of stages can be larger than the word width and that can be used to test an array of RAM modules where the largest RAM word width does not exceed the number of stages of ALU.

ACKNOWLEDGMENT

I express my sincere gratitude to my guide Mrs.ShaikKarimullah for guiding my research work throughout the process and i extend my thanks to annamacharya institute of technology for providing the required lab facilities and promoting this research work.

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