Various Types of Adder comparison based on Power and Area

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Abstract
Addition is used frequently in general purpose computation. Hence multiplication, subtraction and division can be performed using addition. Addition involves a carry ripple step which propagates carry signal from each bit to its higher bit position. This shows circuit delay. The adder lies in the critical delay path determines the system overall speed. We have to focus power consumption of the designed adder is essential. It is extremely important to study the impact of power speed and area while designing the digital systems. Among various adders, the CSA is intermediate regarding speed and area.

I. INTRODUCTION

Over the years wide range of adders have been studied namely Ripple Carry Adder(RCA), Carry Look-Ahead Adder(CLA), Carry Select Adder (CSL), Carry Save Adder(CSA), Carry Skip Adder (CSK) and Conditional Sum Adder (COS). These adders have different structures, size, number of transistors used and power dissipation. Based on the above requirement, we may determine the overall performance.

II. CONSTRUCTION OF ADDERS

Adders are constructed with the help of two basic units named Half Adder and Full Adder. Half Adder adds two binary digits and Full Adder adds two binary digits with carry getting from the previous bit position. This basic unit produces output as sum and carryout. The general form of sum is

$$Sum = A\ XOR\ B\ XOR\ C \text{ and}$$

$$Carry\ = (A\ XOR\ B) AND\ Cin\ OR\ (A\ AND\ B)$$

The above logic can be modified and realize various structures of full adders. The Figure 1 below shows that the logic diagram of 1 bit full adder. These individual adders are group together to realize the n bit adders

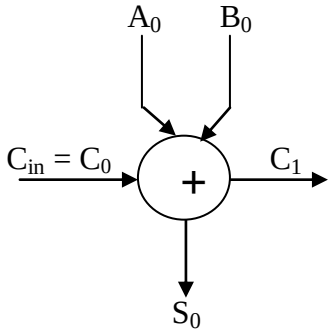

Figure 1: One bit Full Adder

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III. GENERAL DESCRIPTION OF ADDER STRUCTURES

(i) Ripple Carry Adder (RCA)

The basic unit of the Ripple Carry Adder is Full adder. 1 bit Full Adders can be extended to realize N bit RCA. The Figure 2 shows the basic construction of N bit Ripple Carry Adder.

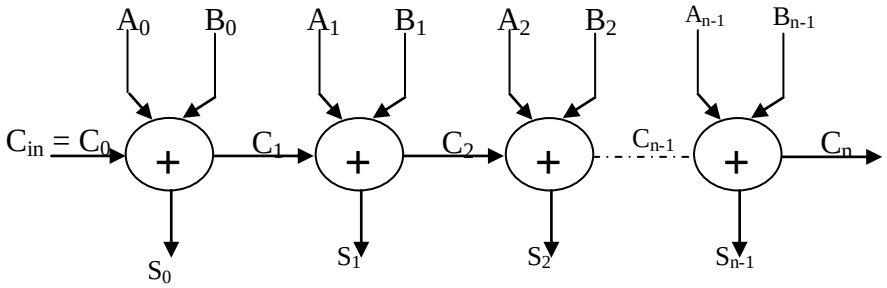

Figure 2: Four bit Ripple Carry Adder

(ii) Carry Look-Ahead Adder (CLA)

It is obvious that Ripple carry adder as size of the input increases the carry–ripple delay grows linearly however these delays can be shortened by generating the carries of each stage in parallel. In the case of Carry Look-Ahead Adder the carry does not depend explicitly on the preceding one. It is expressed as a function of a relevant Propagate and generates Signals namely P_i and G_i and initial carry C_{in}. Hence it has better delay performance at the cost of extra hardware. It is not recommended to use for adder length less than 4.

Generate function $G_i = A_i \,.\, B_i$ and

Propagate function $P_i = A_i$ **XOR** B_i.

The sum and carry for next stage can be defined as

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i \,.\, C_i$$

Where S_i and C_{i+1} are the sum and carry recurrence for i^{th} stage respectively. Since all the carry out are the function of initial carry only the carry for subsequent stage are generated parallel. The 4 bit CLA is shown in Fig 3.

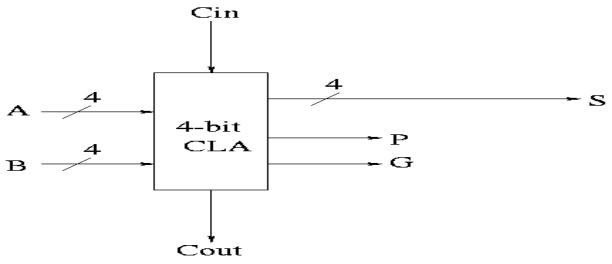

Figure 3: Four bit Carry Look-Ahead Adder (CLA)

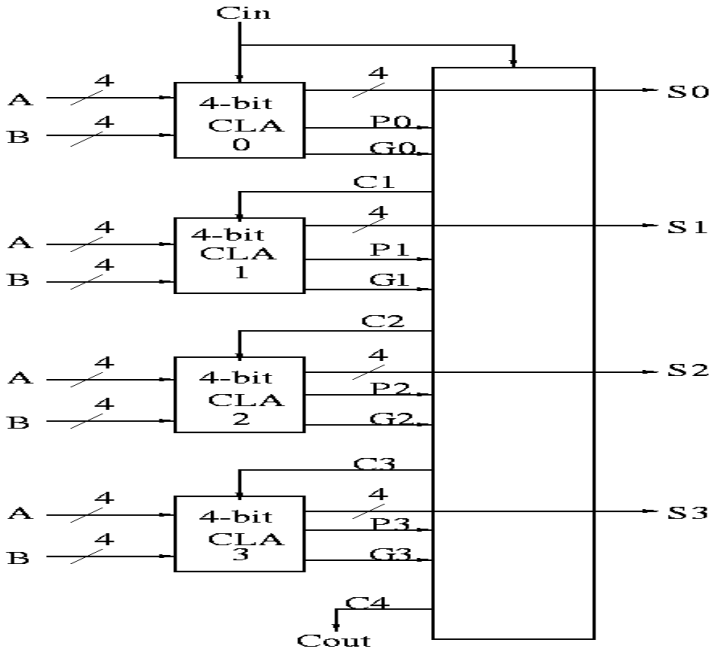

Figure 4: Sixteen bit Carry Look-Ahead Structure

(iii) ***Carry Select (CSA) Adder***

A carry-select adder is divided into sectors, each of which except for the least significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. The 16-bit carry-select adder of Figure 1, for example, is divided into sectors of lengths 1, 2, 3, 4, and 6, proceeding from least-significant to most-significant bit. The 4-bit sector of Figure 4 illustrates the general principle. Within the sector, there are two 4-bit ripple-carry adders receiving the same data inputs but different carry – ins. Adder has a carry-in of zero; the lower

Adder a carry-in of one. The actual carry_in from the preceding sector selects one of the two adders. If the carry-in is zero, the sum and carry-out of the upper adder are selected. If the carry-in is one, the sum and carry-out of the lower adder are selected.
Logically, the result is no different than if a single ripple-carry adder were used. The difference, of course, is in performance. Instead of having to ripple through four full adders, the carry now only has to pass through a single multiplexer.
The carry select adder (CSL) provides a substantial compromise between the RCA which occupies a small area and has a longer delay, and the CLA which occupies larger area and has a short delay. In the CSL both the N bit operands Ai and Bi are divided in to K blocks of possibly different sizes. The figure 5 shows the structure of CSA.

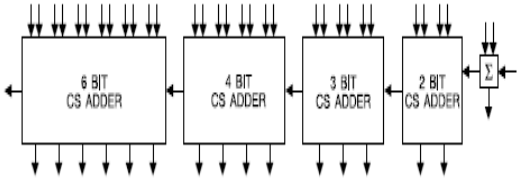

Figure 5: General structure of Carry select adder

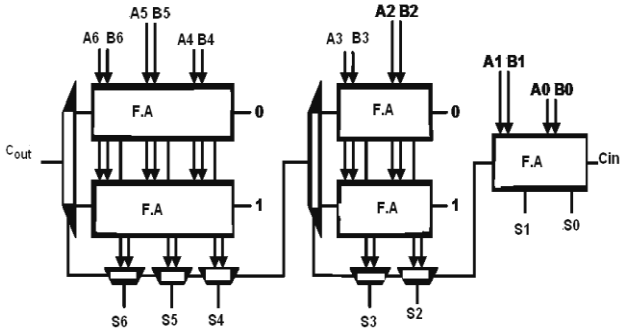

Figure 6: Design flow of CSA

Carry skip adder

Carry skip adder reduces the carry propagation time by skipping over groups of successive adder stages. The carry can skip any consecutive stages if the corresponding bits in the two operands are not equal.

IV. Results and conclusion

The various adders are compared for different parameters like, Silicon area, worst case delay, average power dissipation and Power-Delay product.
An overall performance evaluation and comparison is conducted based on 1.2 micrometer scalable CMOS technology. The table 1 below shows the area and no of transistor required for various adder structures. The RCA occupies the smallest area as compared to other adders however it has the longest worst case delay. The RCA is particularly suitable for applications where the area saving are critical.

Adder type	Area (10^6 λ^2)		No of transistor	
	32 bit	64 bit	32 bit	64 bit
RCA	0.8	1.60	1204	2420
CLA	2.27	4.55	2132	4348
CSL	1.45	2.75	1982	4128
CSA	2.03	3.90	2360	4728
CSK	1.62	3.22	1410	2866

Table 1. Area and No of transistor required

The above mentioned adders are simulated using HSPICE at a power supply voltage of 5 volt. The experiment result obtained using a clock frequency of 10 MHz and is shown in table 2.The delay time is typically considered as the time taken for the carry to ripple from the input to the slowest output, which is from the list significant bit position to most significant bit position.

The Table 2 shows the comparisons of various adders in terms of power dissipation and delay which is the metric for evaluating the performance. Though it is observed from the result that RCA dissipates less power compared to other adder structure however The RCA has the lowest speed because of its long carry chain and therefore not suitable for high speed application. The CSA is the fastest adder and presents the lowest Power delay Product (PDP) which is the most appropriate parameters when analyzing Gate performance.

Adder type	Worst-case delay(ns)		Average power dissipation Per addition in (mw)		Power delay product (PDP)	
	32 bit	64 bit	32 bit	64 bit	32 bit	64 bit
RCA	**55.00**	**109.00**	**0.90**	**1.80**	**49.50**	**197.55**
CLA	15.00	16.50	1.15	2.56	17.25	42.24
CSL	14.50	20.00	1.56	3.31	22.62	66.20
CSA	**4.00**	**4.00**	**1.44**	**2.81**	**5.76**	**11.24**
CSK	22.00	33.75	.98	1.98	21.56	66.85

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Table 2 Comparison of various adder structures for Power, Delay and PDP

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